

Mechanisms for Fatigue and Wear of Polysilicon Structural Thin Films

by

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## **Abstract**

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Fatigue and wear in micron-scale polysilicon structural films can severely impact the reliability of microelectromechanical systems (MEMS). Despite studies on fatigue and wear behavior of these films, there is still an on-going debate regarding the precise physical mechanisms for these two important failure modes.

Although macro-scale silicon does not fatigue, this phenomenon is observed in micron-scale silicon. It is shown that for polysilicon devices fabricated in the MUMPs foundry and SUMMiT<sup>TM</sup> process stress-lifetime data exhibits similar trends in ambient air, shorter lifetimes in higher relative humidity environments and no fatigue failure at all in high vacuum. Transmission electron microscopy of the surface oxides of the samples show an approximate four-fold thickening of the oxide at stress concentrations after fatigue failure, but no thickening after fracture in air or after fatigue cycling *in vacuo*. It is found that such oxide thickening and fatigue failure (in air) occurs in devices with initial oxide thicknesses of ~4-20 nm. Such results are interpreted and explained by a reaction-layer fatigue mechanism; specifically, moisture-assisted subcritical cracking within a

cyclic stress-assisted thickened oxide layer occurs until the crack reaches a critical size to cause catastrophic failure.

Polysilicon specimens from the SUMMiT<sup>TM</sup> process are used to study wear mechanisms in micron-scale silicon in ambient air. Worn parts are examined by analytical scanning and transmission electron microscopy, while temperature changes are monitored using infrared microscopy. These results are compared with the development of values of static coefficients of friction (COF) with number of wear cycles. Observations show amorphous debris particles (~50-100 nm) created by fracture through the silicon grains (~500 nm), which subsequently oxidize, agglomerate into clusters and create plowing tracks. A nano-crystalline layer (~20-200 nm) forms at worn regions. No dislocations or extreme temperature increases are found, ruling out plasticity and temperature-assisted mechanisms. The COF reaches a steady-state value of  $\sim 0.20 \pm 0.05$  after a short time at an initial value of  $\sim 0.11 \pm 0.01$ . Plowing tracks are found before the steady-state value of the COF is reached, suggesting only a short adhesive wear regime. This suggests a predominantly abrasive wear mechanism, controlled by fracture, which commences by the first particles created by adhesive wear.



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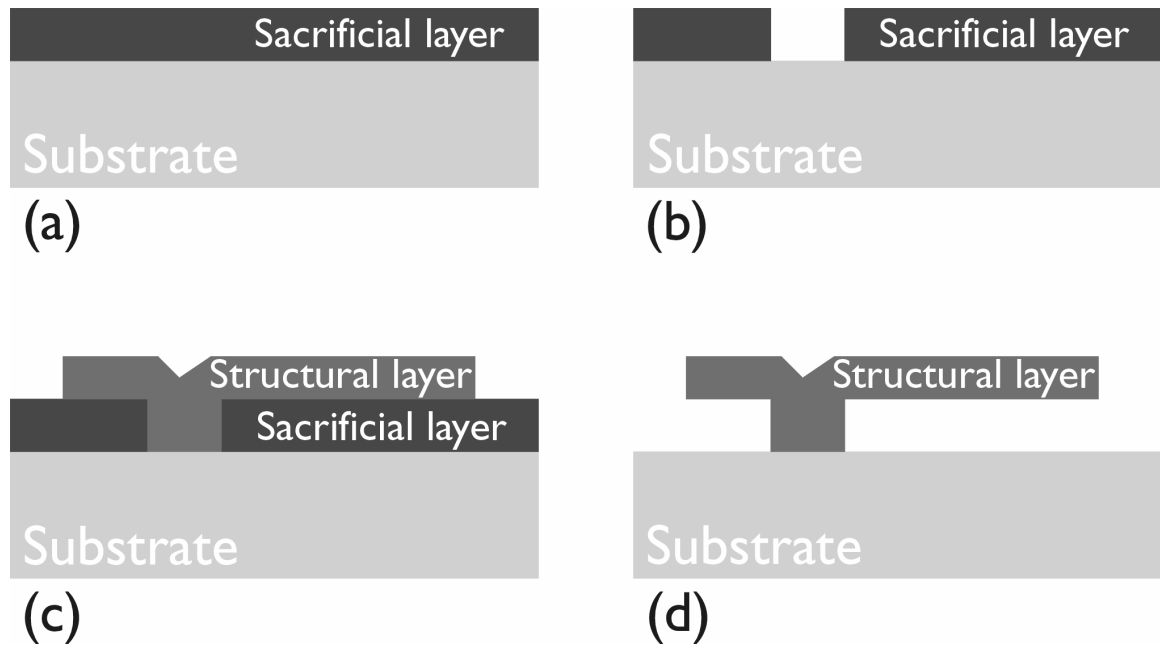
# Chapter 1

## Introduction

### 1.1 Microelectromechanical systems: fabrication and applications

Microelectromechanical systems (MEMS) are small systems with micron-scale features that have both electrical and mechanical components. The mechanical parts of these systems are fabricated using thin film fabrication technologies similar to the fabrication technologies used in the integrated circuit (IC) industry [1]. This allows easy integration of fabrication of electrical and mechanical parts on one chip. Three major steps can be distinguished in the fabrication of MEMS: thin film deposition, patterning and etching. A simple example of a freestanding mechanical structure is given in Figure 1.1, which shows the similarity and difference between MEMS and IC-processing. Starting with a wafer substrate, generally single-crystal silicon, a sacrificial film is deposited (Figure 1.1(a)). This sacrificial layer, often silicon oxide, is removed at the end of the process and is the main difference from IC fabrication where generally no sacrificial layers are used. After deposition the sacrificial layer is patterned, by using an optical mask, using a photoresist layer on top of the sacrificial film and an etching step that removes the sacrificial layer everywhere where there is no photoresist present (Figure 1.1(b)). These steps are repeated for the structural layer: a thin structural film is deposited, patterned and etched (Figure 1.1(c)). To create the free-standing cantilever the sacrificial layer is removed by a wet etch (HF in the case of silicon-oxide) in the final process step (Figure 1.1(d)). Repeating this process numerous times allows the

fabrication of several different types of structures, e.g. cantilevers, suspended masses, gears, springs and hinges, but also more complicated active components such as electrostatic or thermoactuated motors [2]. Because of its abundance, excellent semiconductor properties, high strength and highly developed IC fabrication technologies, silicon is currently the main structural material used in MEMS. A typical sacrificial layer used for silicon based MEMS is silicon oxide, because of its compatibility with silicon during processes and its selectivity during wet etching, allowing the release of the mechanical structures during the removal of this sacrificial layer.



**Figure 1.1:** Schematic illustration of fabrication of a micron-scale cantilever using thin film deposition, patterning and etching (a),(b),(c) techniques similar to those in the integrated-circuit industry. In addition to IC-fabrication, MEMS processes include a release step in which sacrificial layers are removed to create the final free-standing structures (d).

A wide range of MEMS applications, virtually all of them containing silicon structural films, can be found in consumer as well as defense products. Examples are sensors (e.g. pressure, acceleration, gas), gyroscopes, inkjet printer heads, mirror arrays for projectors, optical switches (data transfer, weapon triggering) and micro-needles (e.g. drug delivery) [3]. All these applications have in common that they are both a step forward in miniaturization, making certain applications more portable, but more importantly, they have mass production applications. Because fabrication techniques used in MEMS allow cheap large volume fabrication, there has been great interest in these MEMS applications.

## 1.2 Mechanical reliability issues in MEMS

Despite the growth of the MEMS design field, possible applications, products, and the publication of more system reliability studies over the past decade e.g. [4,5], the number of reliability studies has still been falling far behind that of new MEMS designs, which are getting more and more complicated and demand more from the materials used. According to the MEMS Industry Group [6,7] the prime need of MEMS companies is to acquire a “better understanding of the failure modes and mechanisms” of devices. This need arises because failure modes cannot be observed as easily and because of the large surface to volume ratio of the structures. Therefore, failure modes and mechanisms known from macro-scale material applications cannot automatically be translated to the micron-scale [8,9]. Although silicon is a very strong material ( $\sim 4\text{GPa}$  [10,11]), it is inherently brittle and has relatively low fracture toughness ( $K_{Ic} \sim 1\text{ MPam}^{1/2}$  [12,13]). This strongly affects the performance of silicon as a structural material in MEMS devices in



commercial and defense applications. Along with stiction [8,14], fatigue and wear have been the most important failure mechanism studied in these microsystems so far [8]. Stiction occurs when freestanding MEMS components stick together, impeding motion. This happens by two well defined mechanisms: either during the wet release and drying process step caused by a meniscus (“release stiction”) or during operation when components touch and adhere (“in use” stiction). Several different solutions for this issue have been presented, among which are the use of critical-point drying after removal from the release etch bath and the use of hydrophobic and/or low surface energy coatings. On the other hand, the precise physical mechanisms that cause fatigue and wear in micron-scale silicon structural thin-films have yet to be conclusively determined and will therefore be the focus of this work.

### 1.3 Objectives and experiments

This work will focus on finding the fundamental physical mechanisms causing fatigue and wear in micron-scale polycrystalline silicon (polysilicon) in ambient air. To provide similar loads and other operating conditions as in MEMS devices, the presented experiments are performed utilizing *on-chip* polysilicon MEMS testing devices, electron microscopy techniques for characterization at small length scales and infrared (IR) microscopy, to characterize development of heat during the wear tests.

After a complete review of the literature on fatigue in micron-scale silicon in Chapter 2, the results of the following experiments will be presented in Chapter 3. They will include:

- total lifetime fatigue behavior in ambient air;

- total lifetime fatigue behavior in high relative humidity air;
- total lifetime fatigue behavior in very high vacuum;
- total lifetime fatigue behavior of devices with different post-release oxide layer; thickness (in ambient air as well as in high vacuum)
- damage accumulation measurements;
- and transmission electron microscopy (TEM) study of silicon oxide layers of devices used in all of the type of experiments listed here.

As will become clear in the next two chapters, all these experiments have been designed to address specific points of discussion that exist in the literature and to conclusively determine the mechanism causing micron-scale fatigue in polysilicon.

In Chapter 4, after a short literature review, the following experiments on micron-scale wear of polysilicon in ambient air will be presented:

- scanning and transmission electron microscopy (SEM and TEM) analysis of wear debris and surface for wear;
- energy dispersive X-ray analysis (by SEM and TEM) of wear debris and surface of wear;
- infrared microscopy studies of temperature increases during wear;
- development of the coefficients of static friction as function of the number of wear cycles;
- and SEM characterization of worn surfaces as function of the number of wear cycles.

Similar to the fatigue experiments, this set of experiments has been designed to address current points of discussion in the literature. The data from the experiments listed above

will lead to the proposal of a mechanism explaining micron-scale wear in polysilicon in ambient air. Chapter 5 will recapitulate the most important results and conclusions of the previous chapters and will also discuss future challenges and a few additional experiments that could be conducted with respect to fatigue and wear of micron-scale silicon.

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## Chapter 2

# Fatigue mechanisms in micron-scale silicon structural films

### 2.1 Introduction

The previous chapter has shown that the long-term durability study of micron-scale silicon structures is of particular importance for microelectromechanical systems (MEMS) developers, who heavily use silicon as a structural material. Silicon, however, is quite brittle and subject to several reliability concerns – most importantly, stiction [1,2], wear [1,3] and fatigue – that can limit the utility of silicon MEMS devices in commercial and defense applications. Currently, there are many commercial silicon-based MEMS devices that are subjected to various environments and forms of periodic loading, sometimes at very high frequency, such as resonators found in both radio frequency as well as MEMS sensor applications. Although the maximum operating stresses in these devices are designed to be lower than the fracture stress, delayed failure under cyclic loading may occur for devices that accumulate a large number of cycles over their lifetimes. Because the surface-to-volume ratio of the structural silicon in these devices is very large, traditional failure models developed for materials at the bulk scale cannot always be relied upon to accurately predict behavior, because inherently new physical mechanisms may be operative. Indeed, it is clear that at these size scales, surface effects can control the mechanical properties.

The fatigue behavior of silicon films was first reported in the early 1990s after the testing of micron-scale silicon structures became possible with emerging MEMS technologies. It was quickly discovered by Connally and Brown [4] that the delayed failure under cyclic loading for micron-scale silicon differed from the macro-scale behavior of the material. Silicon is a brittle material that does not exhibit any dislocation activity at low homologous temperatures [5], any extrinsic toughening mechanisms [6], or any evidence of susceptibility to environmentally-assisted cracking [7-9]. Based on this information and knowledge of macro-scale fatigue mechanisms [10], silicon should not fatigue at room temperature and thus the findings of Connally and Brown were both surprising and unexpected. Since that time, there have been several attempts to provide a mechanism capable of explaining this unique fatigue behavior of silicon films.

As will be shown in this chapter, two main classes of mechanisms for fatigue degradation of silicon films currently prevail in the literature. The first class of mechanisms asserts that the fatigue degradation process is a surface phenomenon, in which fatigue of silicon thin films is attributed to a process of subcritical cracking within the surface oxide layer (e.g. [11,12]). Cyclic stress-induced, thickened silicon-oxide reaction layers allow for the initiation and growth of cracks within the layer via environmentally- and cyclically-assisted cracking processes until they reach the critical length where unstable fracture occurs. The second class of silicon fatigue mechanisms that have been proposed asserts that fatigue damage evolves due to subcritical cracking of the silicon itself, rather than the oxide reaction-layer (e.g. [13]). Several causes for this type of crack growth in silicon have been suggested: (i) crack growth due to the cyclic compression fatigue aided by a wedging effect of debris or the oxidized surface inside the

crack; (ii) crack growth occurring by dislocation activity, causing either crack-tip blunting, or crack-tip blunting followed by sharpening (similar to fatigue in ductile materials); or (iii) crack growth caused by grain-boundary deformation by means of plastic (shear) deformation in the thin amorphous region of a grain boundary that intersects the free surface of the film [13]. It will be shown here that based on the results of extensive experimental studies performed using a variety of specimen geometries and testing techniques, mechanisms involving subcritical cracking in the silicon-oxide reaction layers represent the most viable explanation for the phenomena of the fatigue of micron-scale silicon films, and moreover provide a reason why this effect is not seen in bulk silicon.

The numerous studies on both single and poly crystalline silicon are described in the following two sections, including recapitulative (normalized) stress-total lifetime ( $S$ - $N$ ) graphs for fatigue in ambient air. Particular attention is given to the proposed mechanisms for the observed fatigue phenomena and the experimental evidence provided to support these different mechanisms. Details on the various micron- and submicron-scale fatigue testing devices, systems and methods used in this discipline are outlined in Appendix A.

## 2.2 Fatigue testing and mechanisms for single-crystal silicon thin films

In this section, studies on the cyclic fatigue behavior of single-crystal (sub-) micron-scale structural silicon films are described. A compendium of these studies and their principal results are listed in Table 2.1. Factors such as loading conditions, operating

frequency, and environment are shown to contribute by varying degrees to fatigue damage accumulation in thin films, with post-failure material characterization and numerical modeling providing insight for the development of micron-scale silicon fatigue mechanisms.

The micromechanical fatigue testing of silicon thin films began with the work of Connally and Brown on 2.9 and 5  $\mu\text{m}$  thick, single-crystal silicon films in the early 1990s [4,14,15]. Using a notched, electrostatically-actuated resonator system (resonance frequency  $\sim 12$  kHz with a stress ratio of  $-1^1$ ), these authors suggested that delayed failure was caused by water-induced, slow crack growth that occurred by environmentally-assisted cracking in the silica layer that forms on silicon upon exposure to oxygen. In that regard, the fatigue behavior for micron-scale silicon devices did not duplicate macroscopic-scale fatigue, as results from macroscopic silicon specimens clearly show that neither fatigue-crack growth nor environmentally-assisted cracking in air or water occurs in silicon [8,16]. They further observed that the resonator's natural frequency decreased with time, which they interpreted as a measure of subcritical (stable) crack growth; the rate of this frequency change also decreased, which they suggested was associated with a reduction in crack-growth rate with increasing crack length. On the basis of these observations, they proposed that growth rates were rate-limited by the reaction rates at the crack tip or by transport of reaction species to, or from, the crack-tip region. This led them to conclude that the actual mechanism governing crack growth in micron-scale silicon devices (driven at resonance) was more complex than simply environmentally-assisted fatigue of silica [17]. Nevertheless, they strongly believed that

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<sup>1</sup> The stress (or load) ratio  $R$  is defined as the ratio of the minimum to maximum applied stress (or load).

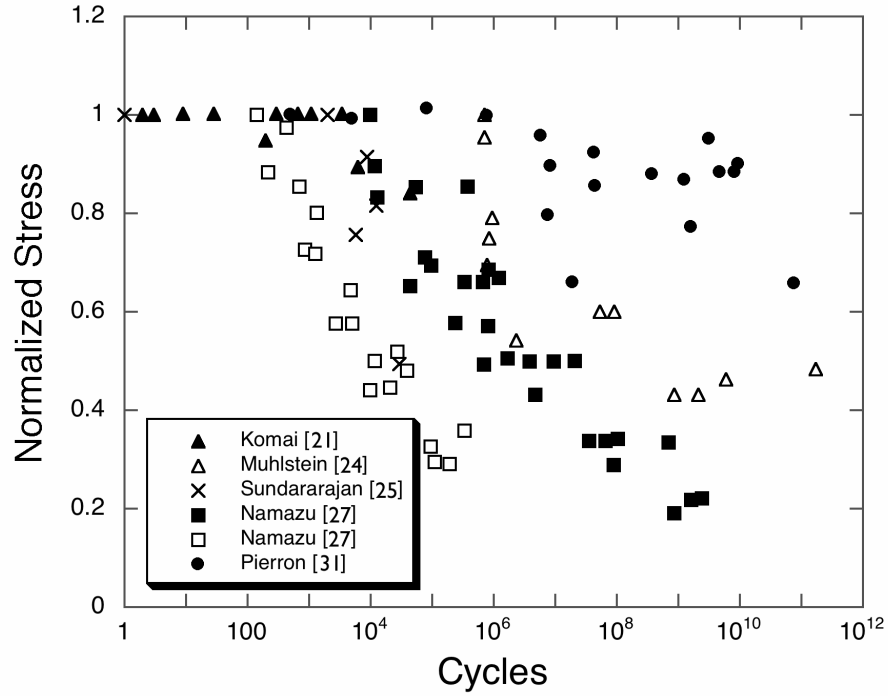


water could accelerate or initiate crack propagation, since while the resonant frequency was observed to remain constant for specimens tested in dry air, a decrease was monitored after introducing wet air into the testing chamber. Fracture surface examination revealed merging of the pre-crack front into a planar front perpendicular to the maximum principal tensile stress, and a change in direction with propagation along  $\{111\}$  low surface energy planes. They postulated that the planar front was due to environmentally-assisted fatigue of the silica layer on the silicon surface. This interpretation of the failure surface should be viewed with some caution since the extent of subcritical crack growth and coalescence of the overdriven pre-cracks in silicon cannot be differentiated fractographically. Furthermore, their quantitative results are somewhat questionable due to the nonlinear behavior of the resonator (which complicates modeling of the system). In spite of these limitations, Connally and Brown were the first investigators to suggest that an inherently brittle material such as single-crystal silicon could undergo cyclic fatigue failure when in the form of a thin free-standing film.

Following this work, several other studies on the fatigue of silicon were conducted. Tabib-Azar *et al.* [18] used a different resonator structure (1.8  $\mu\text{m}$  thick films, resonant frequency around 6-7 kHz,  $R = -1$ ) to correlate damage accumulation and cracking. Their experimental results consisted of measured center frequency and full width at half amplitude (FWHA) of the oscillation spectra. In all the resonators, the FWHA increased with cycling, indicating an increased amount of energy dissipated internally. The changes in FWHA were too large to be caused by thermo-elastic effects, and were therefore postulated to be caused by microcracking of the beam. However, the resonant frequency was found to increase with cycling, a result inconsistent with the

decrease in stiffness associated with microcracking. Moreover, no direct observations of the mode of cracking were made.

Tsuchiya and coworkers confirmed the findings of Connally and Brown, with a study on the influence of environment on the fatigue behavior of single-crystal silicon resonators at 9 kHz (no silicon film thickness specified) [19]. The results of this investigation suggested that the mean fracture strength of the specimen, measured by static loading, was ~17% higher than the mean strength measured by resonant vibration, implying that fatigue occurred over the short number of cycles experienced by the specimen prior to failure. Fatigue failure in air was observed after  $2.9 \times 10^7$  cycles for a specimen initially loaded at a stress 10% lower than the cyclically measured fracture strength and 20% lower for a specimen run for  $1.6 \times 10^8$  cycles. These results revealed that the longer the fatigue life, the more the fatigue damage accumulation, although again no direct observations of this damage were made. Their experimental results did show that the testing environment affected both the specimen's fracture strength and fatigue life. For high humidity environments, mean strengths were 10% lower than for low humidity environments. More recently, Tsuchiya has also shown that in air, the mean fracture strength is 70-80% of the strength *in vacuo* [20]. The fatigue lives were severely reduced for specimens tested in environments containing water vapor and/or oxygen (the effect of water vapor was more pronounced than the effect of oxygen). These authors attributed their findings to a mechanism involving oxidation at a crack initiation site on the silicon surface that allowed further crack growth.



**Figure 2.1:** Normalized applied maximum stress vs. number of cycles to failure ( $S$ - $N$ ) curve for the cyclic fatigue of single-crystal silicon in ambient air taken from the available literature. The stress values are normalized with respect to the stress from the test in that particular study that was run at the lowest number of cycles (and therefore in all but one case also with the test run at the highest stress). For the data from Namazu [27]: the open squares are tests in bending and the closed squares are tests in tension.

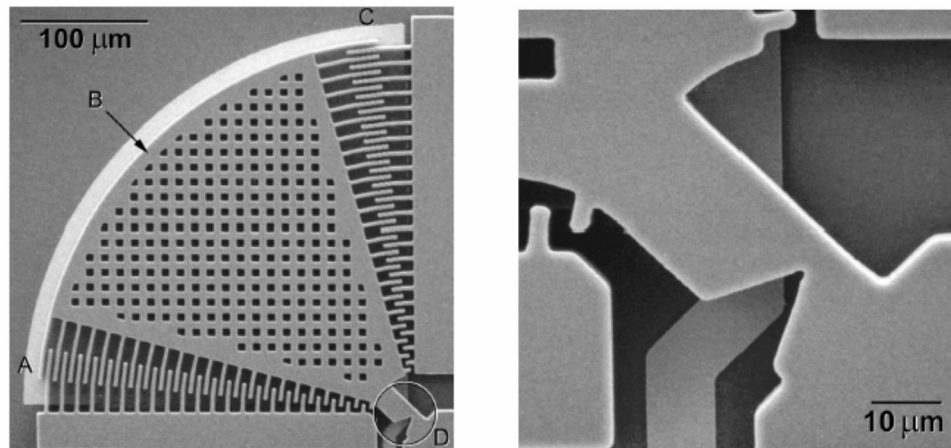
Like Tsuchiya *et al.*, Komai, Minoshima, and coworkers [21,22] investigated the influence of water on the fatigue behavior of 30  $\mu\text{m}$  thick, single-crystal silicon under (near)zero-tension cyclic loading ( $R = 0.1$ ) at a frequency of 0.1 Hz. Komai *et al.* reported shorter fatigue lives in water, compared to air, for a maximum stress of 3.4 GPa (Figure 2.1). In addition, fatigue lives appeared to decrease with increasing immersion time in water prior to testing. Atomic force microscopy (AFM) images of specimens cycled in air did not reveal any nanometer-scale fatigue damage on the specimen surface

after a maximum of  $5 \times 10^4$  cycles. However, nanoscale grooves were observed on fatigued specimens in water using AFM with a sharp tip ( $\sim 5$  nm radius). The orientation of these grooves was not perpendicular to the maximum principal stress, but rather about  $70^\circ$  to the  $\langle 112 \rangle$  longitudinal direction, probably corresponding to cracking along a  $\{111\}$  plane [21,22]. Fracture surface examination of the same sample revealed a crack-initiation site associated with a 300 nm deep defect. Komai *et al.* concluded that a synergistic mechanism of fatigue loading and water environment caused a nanometer-scale crack to develop on a  $\{111\}$  plane and to gradually grow to criticality.

Ando *et al.* [23] also measured tensile loading fatigue effects at  $R = 0.1$  in laboratory air (at 10 Hz) as well as the fracture strength of 5  $\mu\text{m}$  thick silicon thin films. The average quasi-static fracture strain was calculated to be 4.25% in the  $\langle 100 \rangle$  direction and 3.4% in the  $\langle 110 \rangle$  direction, corresponding to fracture stresses of 5.52 and 5.74 GPa, respectively. Under displacement-controlled cyclic actuation, failure occurred after a small number of cycles (ranging from  $10^2$  to  $10^5$  cycles) for maximum applied strains near the mean fracture strain. However, failure was not observed until  $10^6$  cycles or more for applied maximum strains below 75-80% of the average fracture strain. Throughout these displacement-controlled experiments, no decrease in applied load (load resolution  $\pm 1$  mN) was observed during cyclic actuation (maximum load  $\sim 100$  mN), implying that the decrease in stiffness was less than 1% before fatigue failure occurred.

Following up on Brown's earlier work, Muhlstein, Brown, and Ritchie [24] generated stress-life ( $S-N$ ) fatigue curves on 20- $\mu\text{m}$  thick single-crystal silicon films under fully reversed loading conditions ( $R = -1$ ) using a fatigue characterization resonator structure (Figure 2.2) operating in room temperature air at  $50 \pm 2\%$  relative humidity (%)

RH) (Figure 2.1). The fatigue life increased from less than  $10^6$  cycles to more than  $10^{11}$  cycles when the stress amplitude was decreased from 9 to 4 GPa, with no significant effect of frequency (40 vs. 50 kHz). The resonant frequency was observed to decrease monotonically during cycling, suggesting the failure of the silicon thin films occurred after progressive accumulation of damage. Moreover, the longer the life of the specimen, the larger the total decrease in resonant frequency (up to a 25 Hz decrease was observed), again consistent with the notion of damage accumulation. Fracture surface examination revealed a smooth  $\{110\}$  crack path, corresponding to the plane of maximum tensile stress for long-life fatigue specimens, as distinct from the  $\{111\}$  paths observed for single-cycle overload fracture. The authors concluded that a mechanism other than normal  $\{111\}$  cleavage was active during high-cycle fatigue of silicon thin films.

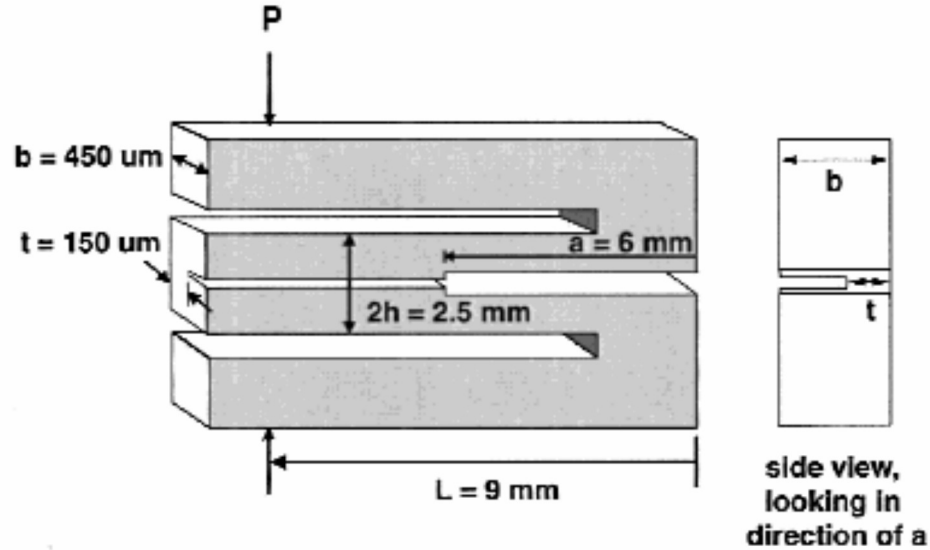


**Figure 2.2:** Scanning electron micrographs of resonator stress-life fatigue characterization structure. The electrostatic comb drive actuator (A), resonant mass (B), capacitive displacement transducer comb (C), and notched cantilever-beam specimen (D) are shown in an overview on the left. A detail of the notched beam is shown on the right.[24]

Sundurarajan and Bhushan [25] were the first to determine the fatigue behavior of nanometer-scale (255 nm thick) single-crystal silicon by collecting *S-N* data (Figure 2.1), as well as the Young's modulus, fracture stress and an estimate of the fracture toughness. The single-cycle bending strength was calculated to be  $17.9 \pm 3$  GPa, a high value attributed to the nanometer-sized specimen. Delayed failure was observed at stresses as low as 6.2 GPa after more than  $3 \times 10^4$  cycles. Scanning electron micrographs suggested that the beams failed by cleavage fracture with a faceted surface for the single-cycle fractured beams, indicating a high-energy fracture on a  $\{100\}$  plane in combination with low-energy cleavage on  $\{111\}$  planes. For the fatigued specimens, smooth fracture surfaces were found, without facets or irregularities. These authors proposed that fracture occurred by low-energy cleavage on  $\{111\}$  planes [25], with a fatigue mechanism similar to environmentally-assisted cracking.

A very large set of *S-N* data was generated by Namazu and Isono at room temperature for nanometer-scale (255 nm thick) as well as micron-scale (2 to 25  $\mu\text{m}$  thick) single-crystal silicon specimens (Figure 2.1) [26,27]. Specimens were run in bending as well as tension, with a positive stress ratio (*R*) and maximum applied cyclic stresses ranging from 10% to 90% of the average fracture strength; the loading frequency was varied from 10 to 450 Hz. In bending fatigue tests, the number of cycles to failure increased from  $10^2 - 10^3$  to  $10^5 - 10^6$  cycles as the peak stress decreased from 90 to 30% of the fracture strength, regardless of the size of the specimen. In tensile fatigue tests, the number of cycles to failure increased from  $10^4 - 10^5$  cycles to  $10^9 - 10^{10}$  cycles as the peak stress decreased from 90 to 20% of the fracture strength, again regardless of specimen

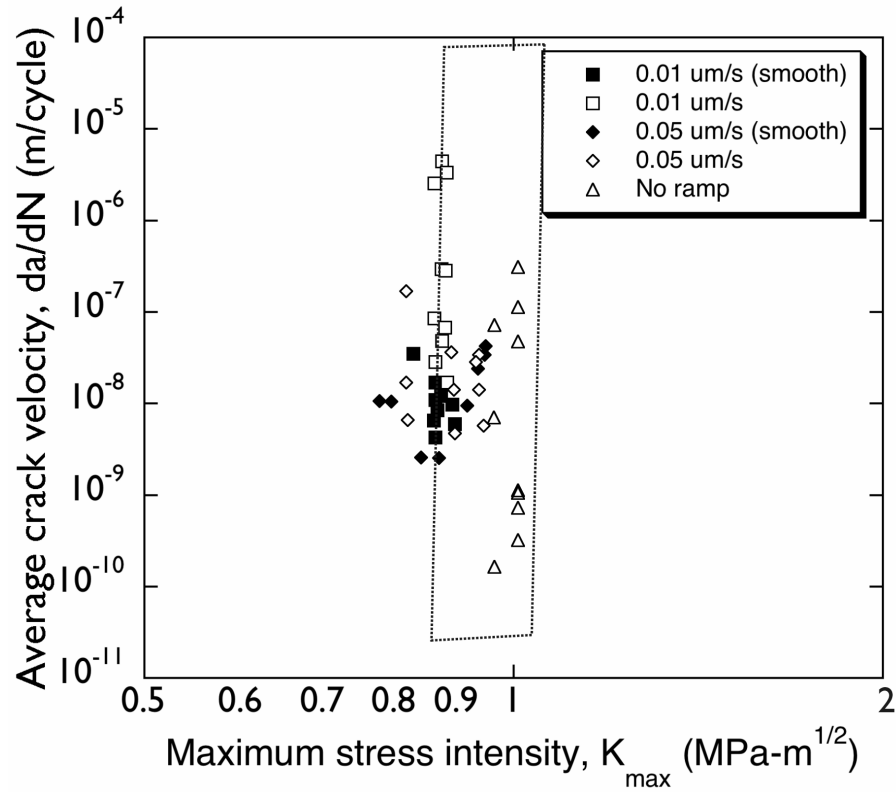
size. No significant influence of the frequency was observed on the number of cycles to failure.



**Figure 2.3:** Schematic illustration of the compression-loaded double cantilever beam specimen. Specimen height is 7.6 mm with a length of 12 mm.[28]

Dauskardt, Kenny, Fitzgerald, and coworkers investigated subcritical crack growth in pre-cracked, 150  $\mu\text{m}$  thick, single-crystal silicon specimens (Figure 2.3) [28,29]. A discrete step-like crack-growth process was observed under monotonic loading. As the load was increased, unstable fracture occurred when the stress intensity,  $K_I$ , approached the toughness of the material (measured at  $K_{Ic} = 1.15 \pm 0.08 \text{ MPa}\cdot\text{m}^{1/2}$ ). Due to the geometry of the specimen,  $K_I$  decreased with crack extension, leading to crack arrest, with the process repeating itself with further loading. Limited evidence of continuous and subcritical crack growth was noted under constant-load conditions, for an applied stress intensity ( $1.05 \text{ MPa}\cdot\text{m}^{1/2}$ ) close to the toughness of the material. The corresponding  $v$ - $K_I$  curves (crack velocity vs. applied stress intensity) suggested that

subcritical cracking only occurred for  $0.9 K_{Ic} < K_I < 0.98 K_{Ic}$ , with a crack-growth rate exponent,  $n$ , higher than 100 (fitting the results to  $v = CK^n$ , where  $C$  and  $n$  are constants). Because subcritical crack growth only occurs in the regime where the applied  $K_I$  approaches the  $K_{Ic}$  value (region III in  $v-K_I$  curves where the crack velocity outpaces transport of the environmental species), the authors concluded that environmentally-assisted subcritical cracking is absent in monotonically loaded micron-scale silicon.



**Figure 2.4:** Fatigue-crack growth data,  $da/dN$  vs.  $K_{max}$ , in 150  $\mu\text{m}$  thick single-crystal silicon (from different load ramps) are compared for cyclic and static fatigue tests. The area marked by the dotted line shows static fatigue test results in 50% relative humidity.[29]

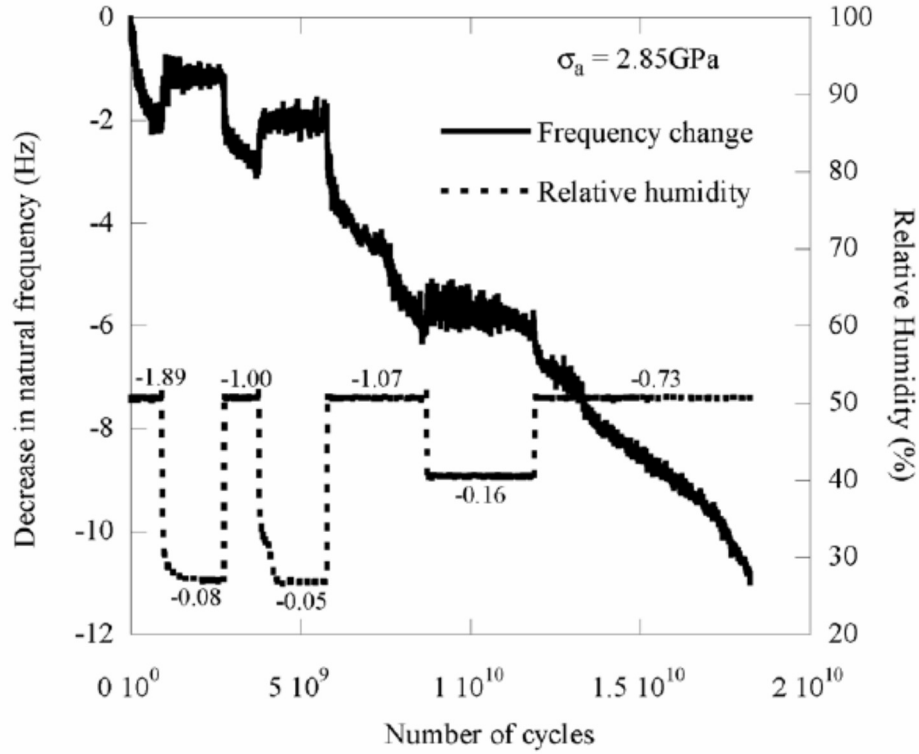


In addition to these quasi-static tests, Dauskardt and co-workers also conducted fatigue-crack growth tests where they cyclically loaded specimens at 20 Hz with nominal stress ratio of  $R = 0.1$ . Akin to monotonic loading conditions, the crack-growth behavior was observed to be step-like in nature, with unstable crack extension when the maximum applied stress intensity reached the fracture toughness. Under decreasing  $K$  conditions, cracks were observed to arrest. The resulting growth rate versus  $K_{\max}$  curves (Figure 2.4) were similar to the curves obtained under monotonic loading, which suggested that the relevant crack-growth process in single-crystal silicon was not true cyclic fatigue. This conclusion was further supported by the fact that fracture surfaces under cyclic and monotonic loading were similar. The authors also conclude that fatigue mechanisms involving cracking of a surface reaction-layer would be a viable mechanism.

Based on the known correlation between damage accumulation in a resonator and its resonance frequency, Koskenvuori *et al.* [30] investigated the long-term stability of micro-resonators in air and vacuum. Four 10  $\mu\text{m}$  thick, single-crystal specimens were tested under resonance for  $4.7 \times 10^{13}$  cycles: two in vacuum ( $P \sim 5$  mbar) and two in air (30 °C, 20-35 %RH). The specimens tested *in vacuo* maintained their initial frequency within 1 ppm (corresponding to a 13 Hz decrease in resonant frequency) after  $4.7 \times 10^{13}$  cycles. In contrast, the resonant frequency ( $f_0$ ) of the specimens tested in air continuously decreased to a total shift of 40-70 ppm from the initial  $f_0$  (i.e., a 550-950 Hz decrease) after  $4.7 \times 10^{13}$  cycles. In addition, a clear correlation between relative humidity and resonant frequency was recorded ( $f_0$  increasing with decreasing %RH). The authors interpreted this result as increased water adsorption at the surface with increasing %RH. They further concluded that the resonator stability could be severely affected by water

contamination of the resonator surface due to the humidity in ambient air. This study provides additional evidence that silicon films degrade over time in air and that this degradation is significantly less in low vacuum.

Most recently Pierron and Muhlstein [31] measured the effect of the service environment on the fatigue resistance of 10  $\mu\text{m}$  thick, single-crystal silicon resonators (resonant frequencies  $\sim 40$  kHz; stress ratio of  $R = -1$ , test sample similar in design to Figure 2.2).  $S$ - $N$  data, incorporated in Figure 1, demonstrated the fatigue susceptibility of these films in ambient air (30  $^{\circ}\text{C}$ , 50 %RH). The fatigue life in air increased markedly from  $5.0 \times 10^2$  to  $7.5 \times 10^{10}$  cycles as the applied stress was reduced from 3.4 to 2.2 GPa. In contrast with the data collected in air, none of the specimens tested in medium vacuum (10-40 Pa) at stress amplitudes between 2.5 and 3.0 GPa failed, at least up to  $\sim 10^{10}$  cycles. Additionally, most specimens tested in air, at stresses higher than 3 GPa, failed before  $10^8$  cycles, whereas for two specimens tested in vacuum, lives exceeded  $10^9$  cycles. Additionally, damage accumulation rates were calculated by monitoring the natural frequency of the resonator during cycling. The surrounding humidity was found to have a dramatic effect on the damage accumulation rate that was one order of magnitude larger at 50 %RH compared to 25 %RH (see Figure 2.5). In contrast, virtually no damage was observed in a medium vacuum environment with a bake performed prior to testing. Fatigue was attributed to a silicon-oxide controlled fatigue mechanism, which suggests moisture-assisted subcritical cracking in a cyclic stress-assisted thickened surface oxide layer. This mechanism will be discussed in more detail in the next section.



**Figure 2.5:** Decrease in resonant frequency,  $f_0$ , during cycling at constant stress amplitude (2.85 GPa) in air (30 °C) at various successive relative humidity levels: 50, 25, 50, 25, 50, 40, and 50 %RH. The numbers near the relative-humidity line indicate the average decrease in  $f_0$  per  $10^9$  cycles for the particular humidity value.[31]

**Table 1:** Summary of fatigue testing of single-crystal silicon thin films from 1991 to 2006. The upwards and downwards pointing arrow-symbols refer respectively to increases and decreases.

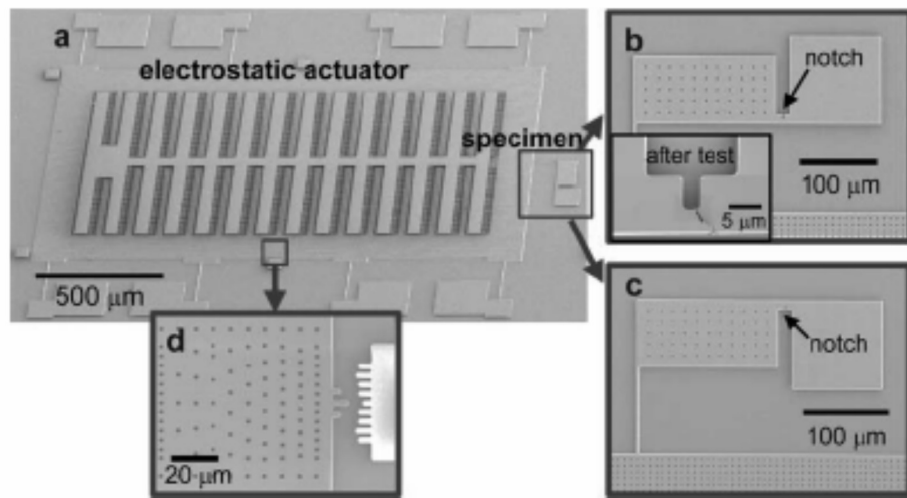
Authors	Specimen Geometry	Actuation Mode / Output Signal Measurement	Frequency $f$ , Stress Ratio $R$	Results
Connally, Brown [4,14,15]	Pre-cracked cantilever beam (16 or 11.5 $\mu\text{m}$ wide, 75 or 130 $\mu\text{m}$ long, 5 $\mu\text{m}$ thick)	Electrostatic actuation at resonance (out-of-plane motion). Capacitive sensing of motion, related to stress via dynamic modeling.	12.3 kHz $R = -1$	$f_0 \downarrow$ during lifetime, at a rate $\downarrow$ with time (wet air, $K \sim K_{Ic}$ ). $f_0$ constant in dry air. Planar crack front $\perp$ to $\sigma_{\max}$ before unstable crack propagation on {111} plane.
Tabib-Azar, Wong, Ko [18]	Cantilever beam (50 $\mu\text{m}$ wide, 600 $\mu\text{m}$ long, 1.8 $\mu\text{m}$ thick)	Electrostatic actuation at resonance (out-of-plane motion). Optical deflection system measuring displacement.	6-7 kHz $R = -1$	Full width at half amplitude $\uparrow$ with cycling. $f_0 \uparrow$ with cycling
Tsuchiya <i>et al.</i> [19,20]	Clamped-clamped beam attached to large mass (1.5x1.5x.5 mm <sup>3</sup> )	Piezoelectric actuator (closed-loop) oscillating specimens at resonance. Strain gage measuring vertical displacement of mass.	$\sim 9$ kHz $R = -1$	Fracture strength $\downarrow$ w/ cycling (even after small number of cycles). Fracture strength and fatigue lives $\downarrow$ as humidity level $\uparrow$ (same with oxygen to a less extent). Fracture strength in air $\sim 75\%$ of vacuum.
Komai, Minoshima, <i>et al.</i> [21,22]	Cantilever beams (45-195 $\mu\text{m}$ wide, 500-2000 $\mu\text{m}$ , 30 $\mu\text{m}$ thick)	Electromagnetic actuator. Displacement measured differential transformer.	0.1 Hz $R = 0.1$	Fatigue lives ( $N_f$ ) in water shorter than in air. $N_f \downarrow$ as pre-immersion time in water $\uparrow$ . Crack initiation site along {111} plane.
Ando, Shikida, Sato [23]	Tensile specimen (50 $\mu\text{m}$ wide, 50 $\mu\text{m}$ long, 5 $\mu\text{m}$ thick)	External loading of <i>on-chip</i> testing device. Load cell and displacement gauge.	10 Hz $R = 0.1$	Failure occurred after $10^2$ - $10^5$ cycles for $\epsilon_{\max} \sim \epsilon_{\text{fract}}$ . No failure after $10^6$ cycles for $\epsilon_{\max} < 80$ -85% $\epsilon_{\text{fract}}$ .
Muhlstein, Brown, Ritchie [24]	Notched cantilever beam (21.5 $\mu\text{m}$ wide, 40 $\mu\text{m}$ long, 20 $\mu\text{m}$ thick) attached to large plate	Electrostatic actuation at resonance (in-plane motion). Capacitive sensing of motion. Visual calibration.	40-50 kHz $R = -1$	Fatigue lives in 50 %RH air $\uparrow$ from $10^6$ to $10^{11}$ cycles by $\downarrow \sigma_a$ from 9 to 4 GPa. $f_0 \downarrow$ during lifetime. Smooth crack path $\perp$ to $\sigma_{\max}$ before crack propagation in {111} plane.
Sundararajan, Bhushan [25]	Nanoscale double-clamped beam (200-800 nm wide, 6 $\mu\text{m}$ long, 255 nm thick)	External load with AFM. AFM load displacement measurement.	4.2 Hz $R > 1$	Fatigue life up to $3 \times 10^4$ cycles at $\sim 30\%$ of fracture strength. Fracture: high energy {100} plane and low energy {111} planes cracking. Fatigue: low energy {111} plane cracking.
Namazu, Isono [26,27]	Nano- and micron-scale fixed-fixed beams + tensile specimens (5-250 $\mu\text{m}$ wide, 36-3000 $\mu\text{m}$ long, 2-25 $\mu\text{m}$ thick; nano, see Sundararajan)	Bending test with AFM or nanoindenter Compact tensile tester Stress-controlled	10-450 Hz $R > 0$	Bending mode: Fatigue lives $\uparrow$ from $10^2$ - $10^3$ to $10^3$ - $10^6$ cycles by $\downarrow \sigma_a/\sigma_f$ from 90% to 30%. Tensile mode: Fatigue lives $\uparrow$ from $10^4$ - $10^5$ to $10^9$ - $10^{10}$ cycles by $\downarrow \sigma_a/\sigma_f$ from 90% to 20%. No influence of frequency on number of cycles to failure.
Fitzgerald Kinney, Dauskardt <i>et al.</i> [28,29]	Compression-loaded double cantilever-beam specimen (pre-cracked, 150 $\mu\text{m}$ thick)	External loading. Crack growth measured from ohmic drop measurements in deposited Ti film. $K = f$ (load, crack length)	20 Hz $R = 0.1$	No true stress-corrosion cracking observed from calculated $v$ - $K$ curves. No true mechanical fatigue-crack growth process observed.
Koskenvuori <i>et al.</i> [30]	Resonator arm (145 $\mu\text{m}$ long, 10 $\mu\text{m}$ thick)	Electrostatic actuation (length-extensional mode). Frequency response w/ network analyzer in transmission mode	13.1 MHz $R = -1$	$f_0$ constant within 1 ppm after $4.7 \times 10^{13}$ cycles at 5 mbar; $f_0 \downarrow$ by 40-70 ppm in lab air. Clear correlation between %RH and $f_0$ changes ( $f_0 \uparrow$ as %RH $\downarrow$ ).
Pierron, Muhlstein [31]	Notched cantilever beam ( $\sim 20$ $\mu\text{m}$ wide, 40 $\mu\text{m}$ long, 10 $\mu\text{m}$ thick) attached to large plate	Electrostatic actuation at resonance (in-plane motion). Capacitive sensing of motion. Visual calibration.	$\sim 40$ kHz $R = -1$	Fatigue lives from $5 \times 10^2$ to $7.5 \times 10^{10}$ with stresses from 3.4 to 2.2 GPa in air. No failure <i>in vacuo</i> after $10^{10}$ cycles. $f_0 \downarrow$ during lifetime in air; $f_0$ constant in vacuum with bake. $\Delta f_0/\Delta t \uparrow$ as %RH $\uparrow$ .

## 2.3 Fatigue testing and mechanisms for polycrystalline silicon thin films

After the initial publications on fatigue in single-crystal silicon films, results on polycrystalline silicon structural thin films soon became available. These are reviewed below, again in chronological order, with a compendium listed in Table 2.2. In general, they demonstrate that factors such loading conditions, operating frequency and, most importantly, environment have effects that are similar to those described above for single-crystal silicon.

Early work on fatigue in polycrystalline silicon (polysilicon) films, by Van Arsdell and Brown [32], used a polysilicon fatigue testing resonator (resonant frequency  $\sim 40$  kHz, stress ratio  $R = -1$ , similar to Figure 2), comprising a  $2\text{ }\mu\text{m}$  thick, pre-cracked cantilever-beam sample. Akin to studies on single-crystal silicon thin films, results showed a susceptibility of micron-scale polysilicon to delayed fracture by fatigue. In wet air, a decrease in resonant frequency of the pre-cracked specimens was observed and interpreted as crack growth (the calculated maximum applied stress intensity was  $\sim 0.3\text{ MPa}\cdot\text{m}^{1/2}$ ); in dry air, the resonant frequency did not change significantly. To confirm that the decrease in frequency was related to damage at the crack tip, uncracked (control) specimens were tested and showed no resonant frequency changes in wet air. Based on these studies, the authors concluded that polysilicon thin films were susceptible to subcritical crack growth via an environmentally-assisted cracking mechanism. Fracture surface examination suggested a transgranular crack path, which was considered as further proof of environmentally-assisted cracking involving the native oxide film rather than the polysilicon itself. The authors argued that the environmentally-assisted cracking

mechanism in the oxide would repeat itself, as the reduced diffusion path for further oxidation (due to cracking) would facilitate further growth of the oxide film at the crack tip. They referred to this as “static fatigue”, as it only seemed to depend on the environment and stress level, even though no experimental data were obtained under static loading. This mechanism excludes the effect of the number of load cycles on the observed fatigue behavior; this in contrast to the silicon-oxide controlled fatigue mechanism suggested by Muhlstein *et al.* [11], which also attributes the fatigue effect to cracking in the surface oxide layer, as discussed later in this section.



**Figure 2.6:** Scanning electron microscopy (SEM) images of a micromachined device for measuring bend strength and fatigue resistance. (a) The electrostatic comb-drive actuator integrated with the fracture mechanics specimen. (b,c) Higher magnification rotated images of two single edge-notched fatigue specimens that can be integrated with the actuator; the inset in (b) shows the notch area after testing. (d) Higher magnification rotated image of the measurement scale used for optical displacement detection.[36]

Completely different mechanisms for the fatigue of micron-scale polysilicon were suggested by Kahn, Ballarini, Heuer and coworkers [13,33-35], based on results from specimens (Figure 2.6) tested at varying stress ratios ( $-3 < R < 0.5$ ) in laboratory air and in a medium vacuum (8 Pa pressure). Compared to average monotonic strengths for boron-doped and undoped polysilicon specimens of, respectively, 4.1 and 4.9 GPa, the mean strengths of these specimens driven at resonance (10 kHz) and quickly ramped ( $\sim 2000$  to  $10^5$  cycles) to failure was 3.2 and 4.1 GPa, implying a significant decrease in strength due to short-time ( $< 10$  sec) cycling.<sup>2</sup> High-cycle fatigue failure was observed in air after  $\sim 10^9$  cycles at a maximum tensile stress of roughly half the monotonic strength. Fracture surface examination revealed a semi-circular “mirror” localized along the thickness of the specimen; this is typical of brittle fracture and characteristically surrounds a crack-initiating flaw. Kahn *et al.* claimed that fatigue crack initiation and growth occurred during cyclic loading in both air and vacuum, although the process was faster in air. They also suggested that mechanical damage could occur during the tensile-compression cycles, specifically in the form of microcracks. This represented a purely mechanical mechanism for the fatigue behavior of silicon thin films via subcritical cracking of the silicon itself. The notion of mechanical damage in silicon was preferred by Kahn *et al.* to an environmentally-assisted cracking because they could not observe static fatigue, as suggested by Van Arsdel and Brown [32], in their silicon thin films. Using pre-cracked, doubly-clamped 3 and 3.7  $\mu\text{m}$  thick silicon beams, with residual tensile stresses  $\sim 50$  MPa, no subcritical crack growth was observed under sustained (non-

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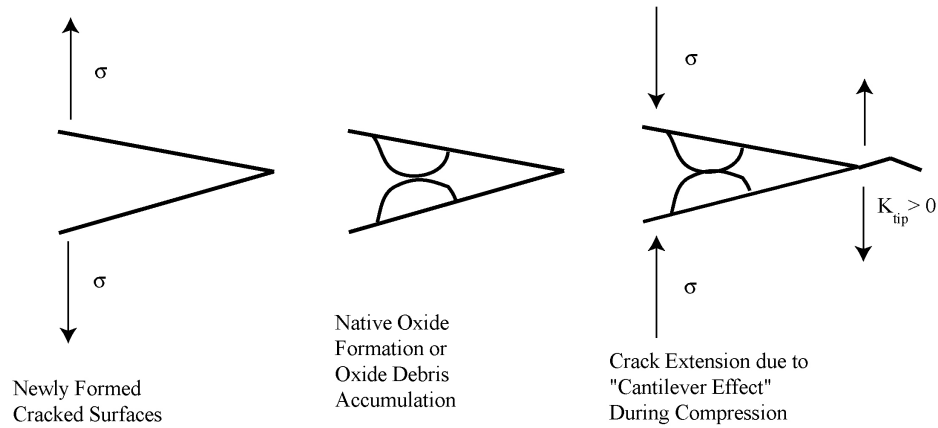
<sup>2</sup> The term “low-cycle fatigue” can be used here as these results refer to a test in which the stress amplitude is ramped until failure while the specimen is resonating. Most *S/N* fatigue tests of thin-film silicon, however, are carried out under “high-cycle fatigue” conditions, where high-cycle, nominally constant amplitude cycling is performed until specimen failure, as described in Appendix A.

cyclic) loading (constant stress of 3.6 GPa) in laboratory air or wet (90 %RH) air. These authors further found that the low-cycle fatigue strength of the electrostatically-actuated single edge-notched micro-specimens was affected more by the stress ratio (or equivalently by the maximum compressive stress) than by the environment [34]. On the basis of this observation, they concluded that the fatigue mechanism for silicon thin films was strongly affected by the compressive portion of the loading cycle, which they reasoned could either create a micro-crack at the surface due to wedging on surface asperities, and allow further crack growth due to a mechanism similar to far-field cyclic compression fatigue of brittle ceramics [36]. They also investigated the high-cycle ( $1 \times 10^4$  to  $3 \times 10^8$  cycles) fatigue behavior in air and vacuum, and found no fatigue failures in a medium vacuum [34], from which they concluded that ambient air exacerbated the cyclic compression fatigue mechanism. To account for their observations, Kahn *et al.* postulated that thickened surface oxide on newly formed crack surfaces in air could cause wedging effects that would create additional subcritical cracking (Figure 2.7), or that wear debris formed in vacuum could prevent crack closure and therefore decrease crack-driving force and growth (Figure 2.8) [35].

The feasibility of this latter mechanism, i.e., that surface debris and/or oxidation can induce “cantilever effects” to drive the crack, has been recently questioned by Pierron and Muhlstein [37]. Utilizing a fracture-mechanics based finite-element model, they calculated the crack-opening profile and the driving force for advance of wedged cracks, and found that in compression, such wedges do not cause an increase of the magnitude of the stress-intensity factor. It is thus unlikely that this mechanism contributes significantly to the fatigue of silicon thin films. Furthermore, arguments based on the role of



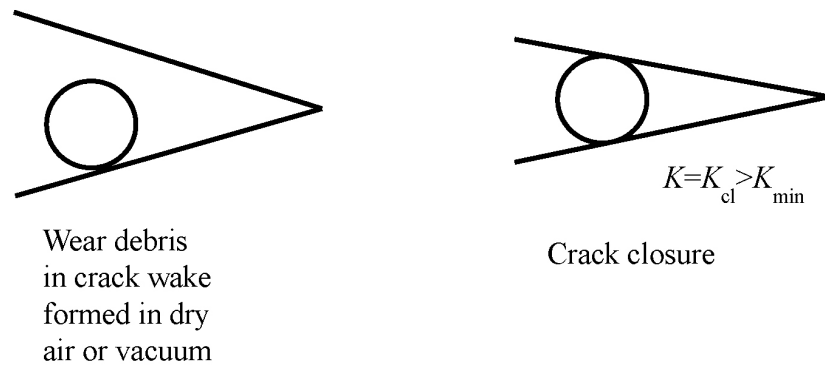
compressive loading fail to account for observations of fatigue failure in silicon films under cyclic tension loading (i.e., at  $R \geq 0$ ) [13,21-23,25-29,33-35].



**Figure 2.7:** Schematic illustration of the mechanism, proposed by Kahn *et al.*, to explain the influence of environment on the fatigue behavior of silicon thin films. In air, native oxide formation or oxide debris accumulation creates local wedges within the wake of newly formed crack surfaces. Under compression loading, the wedge is assumed to create a driving force for further crack extension due to a “cantilever effect”.[36]

The effect of mean stress and stress amplitude on the low-cycle fatigue of 5.7  $\mu\text{m}$  thick B-doped polysilicon was studied by Kahn *et al.* [13]. Their results showed that for samples loaded with an increasing amplitude cyclic stress, with a positive mean stress the fracture stress was higher, whereas with negative mean stress the fracture stress was lower. They found that this was consistently the case for both Pd-coated undoped as well as B-doped specimens in air as well as medium vacuum (10 Pa), although the slope in the fracture stress vs. mean stress plot was different. From these data, they concluded that cyclic, and not monotonic, loading does have an influence on the fracture stress. They further showed data from tests where specimens were loaded with an applied cyclic

stress, with mean stress offset, below the fracture stress, followed by a ramp to failure. For Pd-coated undoped specimens with a compressive mean stress of 2.2 GPa, the monotonic fracture strength decreased with higher cyclic amplitudes, particularly at cyclic amplitudes greater than 3 GPa. At a cyclic amplitude of 2 GPa, conversely, B-doped specimens showed an increase in monotonic strength, as compared to non-cycled specimens, independently of whether the mean stress was tensile or compressive. These low-cycle fatigue results were rationalized in terms of a “weakening and strengthening map” (Figure 2.9), where weakening occurs when the fatigue amplitude is high and the mean stress is high, or low when compressive or low when tensile. Strengthening is found at low fatigue amplitude where the mean stress is highly compressive or highly tensile. No effect is found at low fatigue amplitudes with low mean stress (compressive or tensile).



**Figure 2.8:** Schematic illustration of the influence of environment on the fatigue behavior of silicon thin films proposed by Kahn *et al.* Wear debris formed in dry air or vacuum accumulate in the crack wake, leading to crack closure.[36]

Fatigue amplitude	High	weakening		weakening	(not measured)
	Low	strengthening	no effect	no effect	strengthening
		High	Low	Low	High
		Mean stress			

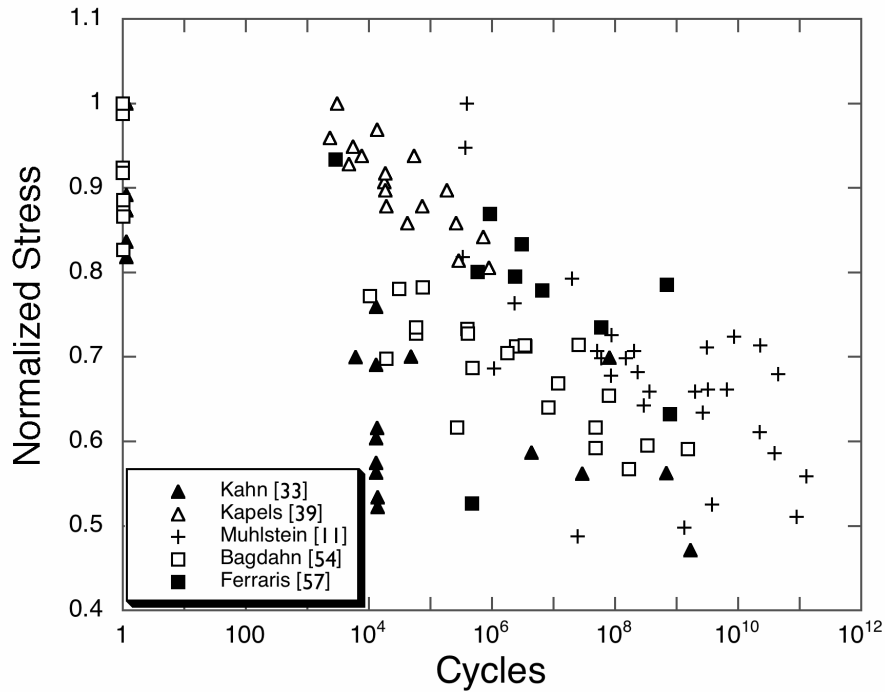
**Figure 2.9:** Qualitative weakening/strengthening map showing the influence of the fatigue amplitude and mean stress.[13]

To account for these “weakening” and “strengthening” effects, Kahn *et al.* suggest three possible fatigue mechanisms. The first of these involves microcracking of the silicon; they argue that this would account for the weakening, and also for the strengthening due to crack-tip shielding, although they admit that this explanation is “unappealing”. A second mechanism was suggested involving dislocation activity, which would cause crack-tip blunting in the case of a strengthening effect and crack-tip blunting followed by sharpening for a weakening effect. They cite evidence for this mechanism that such dislocation motion has been reported for indentation experiments at room temperature, and that the loading conditions for small fatigue amplitudes and high compressive mean stresses would present similar shear stresses; however, observations of room temperature dislocation plasticity in silicon show a substantial residue of dislocations in the strained area after unloading – for a similar mechanism to be operative during fatigue there should be a readily detectable dislocation density observed in the silicon itself. This has not been found in the studies to date [11,13]. The reason for this

high dislocation density is that at room temperature, dislocations do not move by thermally-activated kink motion, but rather by stress-assisted kink motion. Upon removal of the load, the dislocations are 'frozen' into the structure, and are thus readily observable. Additionally, there has been no direct evidence to date (e.g., from transmission electron microscopy (TEM) imaging) where dislocations have been seen at arrested crack tips in silicon; room-temperature dislocation plasticity in silicon has only been observed to date during the high combined compressive and shear loads of an indentation test [38]. Their third possible mechanism involved grain-boundary plasticity, where an amorphous grain-boundary region hitting the surface under stress would experience a non-conventional plastic deformation in shear, which would then cause a residual compressive stress, possibly resulting in the observed strengthening effect. Kahn *et al.* presented a finite-element model to show that with such grain-boundary plasticity residual compressive stresses could occur (independently of the fact of the applied mean stress is compressive or tensile). Varvani-Farahani [39] suggested a related type of mechanism based on modeling of cyclic slip of silicon. However, theories based on cyclic slip in silicon have no physical basis below the ductile-to-brittle transition temperature [5] and their claimed ability to "predict" a stress-life fatigue curve is based on an n-parameter curve fitting, which, should not be construed as an indication of mechanistic accuracy. No experimental evidence for both of these modeled results exists; furthermore, the fact that single-crystal micron-scale silicon is also susceptible to fatigue failure is totally inconsistent with any mechanism involving only grain boundaries. Most importantly, these mechanisms do not account for the fact that fatigue is not observed in macro-scale silicon; moreover, purely mechanical mechanisms are inconsistent with the

definitive effect of environment found in many thin-film silicon fatigue studies [19,20,21,30,31].

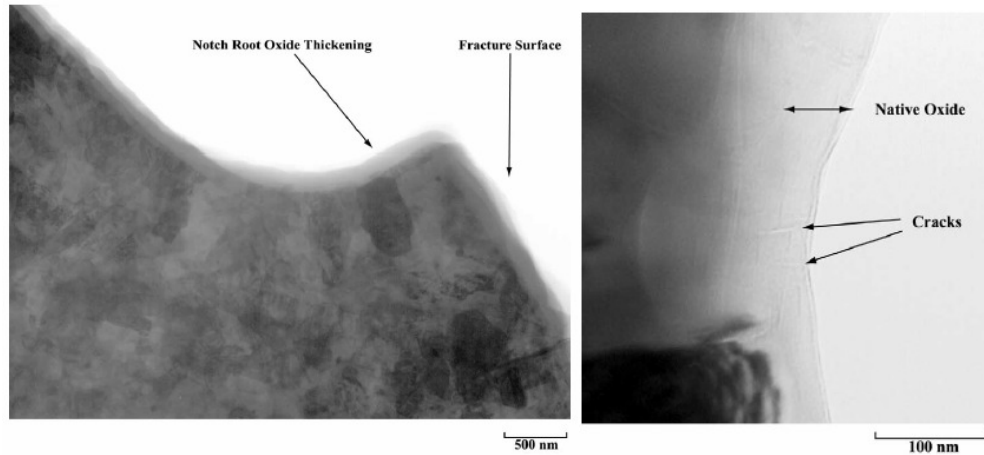
Stress-life fatigue data were also reported by Kapels, Aigner and Binder [40] on 4  $\mu\text{m}$  thick polysilicon. These authors used Weibull statistics to determine a mean fracture strength of their tensile specimens of  $2.9 \pm 0.5$  GPa, with a Weibull modulus of  $6.4 \pm 1$ . Additionally, their  $S$ - $N$  fatigue data indicated delayed failure after cyclic loading, at 1 Hz at  $R = 0$ , for maximum stresses below the mean fracture strength; fatigue lives were increased with decreasing maximum stress. Fatigue failure was observed after  $10^6$  cycles for a maximum tensile stress of 2.2 GPa (Figure 2.10).



**Figure 2.10:** Normalized, applied maximum stress vs. number of cycles to failure ( $S$ - $N$ ) data for fatigue of polysilicon in ambient air. The stress values are normalized with respect to the stress from the test in that particular study that was run at the lowest number of cycles (and therefore in all but one case also with the test run at the highest stress).

More recently, Muhlstein *et al.* [11,41-43] presented extensive stress-life fatigue results for 2  $\mu\text{m}$  thick polysilicon films (fabricated at the MEMSCAP Multi User MEMS Process (MUMPs) Foundry [44,45]), where they observed an increase in fatigue life from  $\sim 3 \times 10^5$  to  $1.2 \times 10^{11}$  cycles by decreasing the sinusoidal stress amplitude from 4.0 to 2.0 GPa (Figure 2.10); these tests were performed at  $\sim 40$  kHz at  $R = -1$ , using a resonating cantilever-beam system similar to that shown in Figure 2.2. Fatigue failure was accompanied by a monotonic decrease in resonant frequency during cycling, which was interpreted as fatigue damage accumulation, specifically in terms of subcritical cracking and oxidation [46]. From these results, a detailed mechanism for thin film silicon fatigue was proposed by Muhlstein, Stach and Ritchie [11,42] based on the notion of reaction-layer fatigue, which involves moisture-induced stable cracking in the thickened oxide layer. Evidence for this was found in high-voltage transmission electron microscopy (HVTEM) images of control specimens, fatigued specimens, and specimens interrupted prior to failure, which revealed striking differences in the surface oxide found at the notch root [11,42]. A native surface oxide of  $\sim 30$  nm in thickness was uniformly distributed over the surfaces of the control samples. In contrast, the surface oxide layer was significantly thicker (up to 90 nm) at the notch root of fatigued specimens (Figure 2.11). In addition, HVTEM images of intact specimens that experienced a large number of cycles also revealed several stable small cracks within the thickened surface oxide, indicating the presence of subcritical crack growth (Figure 2.11). High-resolution infrared imaging of the fatigue specimen revealed only minimal temperature changes ( $\sim 1\text{K}$ ) during testing, which strongly implied that the enhanced notch root oxidation was not thermally induced but mechanical in origin [11]. As discussed below, since the cracking

processes occurs within the oxide layer, this mechanism is consistent with the fact that bulk silicon is not susceptible to environmentally-induced cracking in air [9,16,28,34].

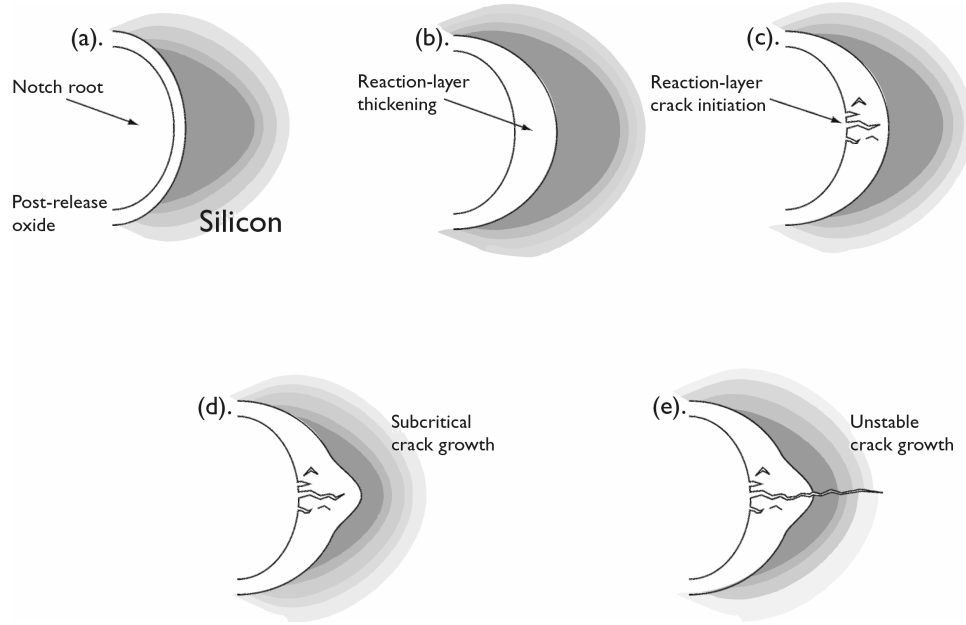


**Figure 2.11:** HVTEM images of the notch region in an unthinned, 2  $\mu\text{m}$  thick, polycrystalline silicon test sample after high-cycle fatigue. (left) This image shows enhanced oxidation at the notch root that failed, after  $3.56 \times 10^9$  e cycles at stress amplitude of  $\sigma_a = 2.26$  GPa. (Right) This image shows stable cracks,  $\sim 50$  nm in length, in the native oxide formed during cyclic fatigue loading; testing of this sample was interrupted after  $3.56 \times 10^9$  cycles at a stress amplitude  $\sigma_a = 2.51$  GPa. Image was intentionally defocused to facilitate the observation of the cracks.[11]

In light of these results, the fatigue of silicon thin films was attributed to a mechanism of sequential, cyclic stress-assisted oxidation and environmentally-assisted cracking of the surface oxide layer that forms upon exposure to moisture- and/or oxygen-containing atmospheres, a mechanism that was termed reaction-layer fatigue (Figure 2.12). The decrease in natural frequency of the fatigue characterization structure during testing, caused by a change of compliance of the resonator and measured using capacitive sensing, was found to be consistent with quantified damage evolution (using finite-element modeling) in the form of oxide thickening ( $-0.5$  Hz per nm of oxide growth) and subcritical crack growth ( $-1$  Hz per nm of crack extension) within the oxide

(Figure 2.13) [11,41]. In particular, the maximum crack extension deduced from resonant frequency changes was found to be similar than the calculated critical crack size (through numerical modeling) and less than the observed surface oxide layer [43]. This implied that the entire process of fatigue crack initiation, growth and the onset of final failure of the entire structure occurred within the oxide layer. Since the crack in the oxide layer must cause failure of the entire structure, the criterion for this mechanism is that the thickness of the oxide layer,  $h$ , must be greater than or equal to the critical crack size,  $a_c$ , to fail the entire structure, i.e., when  $a_c < h$ . Because the oxide layer thickness in bulk silicon will only be a tiny fraction of the material, the beauty of this mechanism is that it provides an explanation as to why no delayed failure would occur by fatigue in bulk silicon as a growing crack in the oxide layer could never get large enough to break the entire structure i.e., as  $a_c > h$ . Using a fracture-mechanics analysis, Muhlstein and Ritchie [43] defined the range of oxide thicknesses where reaction-layer fatigue would be viable; their calculations suggested that a oxide thickness of ~50 nm was required. Subsequent work by Pierron and Muhlstein [47] expanded this numerical model to account for an alternative failure scenario where stable crack growth in the oxide changes to unstable crack growth when the crack hits the silicon/oxide interface, i.e., when  $a_c = h$ ; this lowered the oxide thickness that is potentially susceptible to reaction-layer fatigue to ~15 nm. The mechanism also explained the decreasing growth rates observed for cracks propagating within the oxide layer; as these cracks approach the SiO<sub>2</sub>/Si interface (with its three-fold modulus mismatch), fracture-mechanics calculations of the crack-driving force showed that it decreased as cracks got closer to the interface [43].

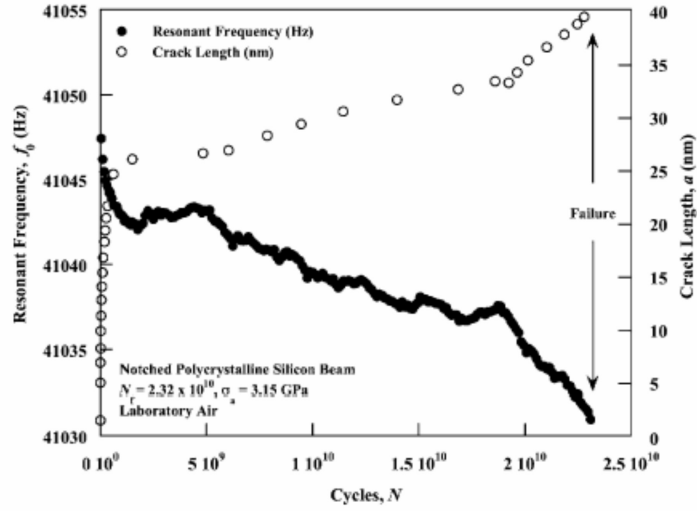




**Figure 2.12:** Schematic illustration of the reaction-layer fatigue mechanism for thin-film fatigue at the notch of the polycrystalline silicon cantilever beam: (a) reaction layer (post-release oxide) on surface of the silicon, (b) localized cyclic stress-assisted oxide thickening at the notch root, (c) moisture-assisted crack initiation in the surface oxide at the notch root, (d) additional thickening and cracking of reaction-layer, and (e) unstable crack growth in the silicon film.[11]

One puzzling aspect of these studies was the thick post-release oxide layers found on the MUMPs [44,45] fabricated fatigue samples studied by Muhlstein *et al.* [11,41,42]; whereas native oxides on the order of a few nanometers thick are expected for polysilicon films, the initial oxides on the MUMPs samples were 20 nm or more. Pierron *et al.* [48] examined this phenomenon and found that these relatively thick oxides can be formed at room temperature during “release”, i.e., chemical removal of the silica layer in an HF bath, due to a galvanic effect between the n+-type silicon and gold (the polysilicon MUMPs process has a gold deposition step [45]). The growth of these surface oxides in concentrated HF solutions, that are usually associated with oxide dissolution, was predicted from the measured current-density/voltage behavior and the geometry of

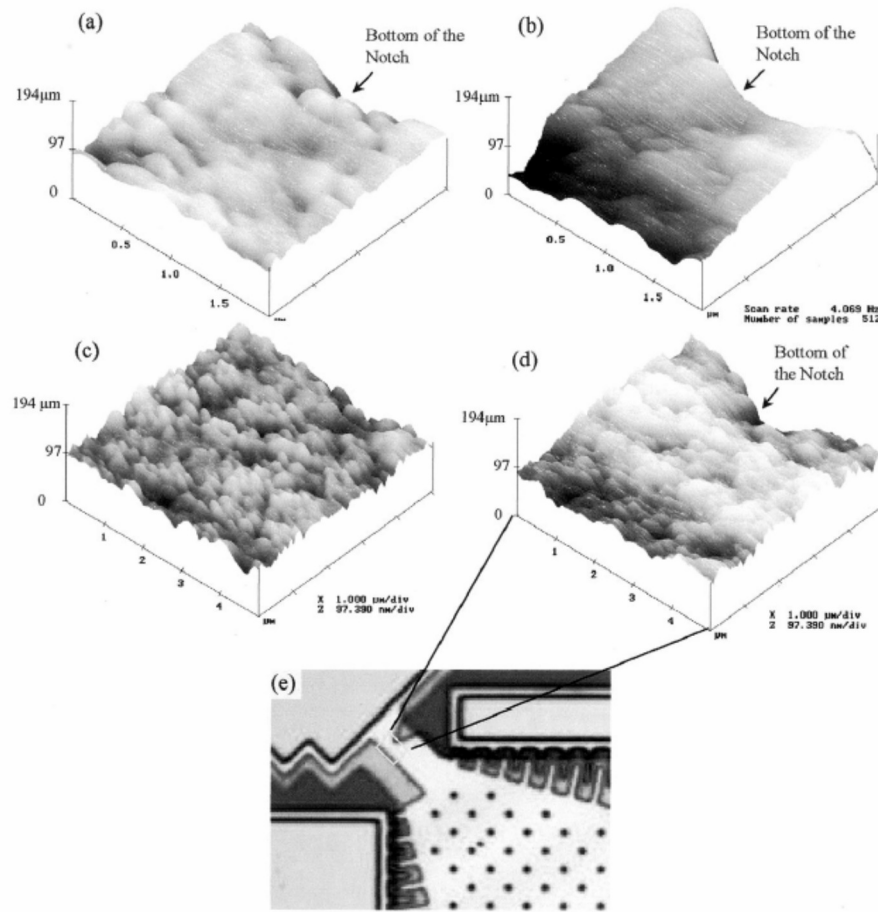
the galvanic couple, and verified by Auger electron spectroscopy measurements. This explanation for thickened post-release oxide layers in MUMPs processed MEMS was later confirmed by Kahn *et al.* [49].



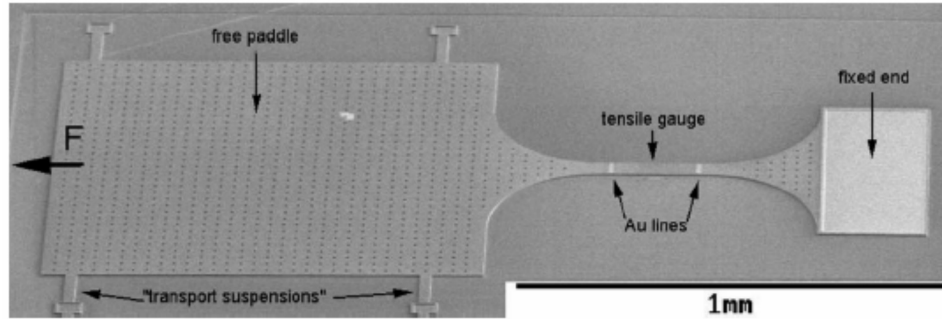
**Figure 2.13:** Representative damage accumulation in polycrystalline silicon, shown by experimentally measured decrease in resonant frequency,  $f_{\text{crack}}$ , with cycles during a fatigue test ( $N_f = 2.23 \times 10^{10}$  cycles at  $\sigma_a = 3.15$  GPa) and the corresponding computed increase in crack length,  $a$ . [11]

A complementary mechanism to reaction-layer fatigue was proposed by Allameh, Soboyejo, and coworkers [12,50-52], who studied the evolution of surface morphology of polysilicon MEMS during cyclic actuation, using the same fatigue resonators as Muhlstein *et al.* (Figure 2.2). *In situ* AFM images of the region near the notch, before and after cyclic actuation at a stress amplitude of 2.7 GPa for  $2 \times 10^9$  cycles, revealed definitive changes in surface topology (Figure 2.14). Specifically, the measured roughness of the surface in the immediate vicinity of the notch was found to increase after cycling from 10 to 20 nm. The roughness changes diminished with increasing distance from the notch, indicating a role of stress in the evolution of surface topography

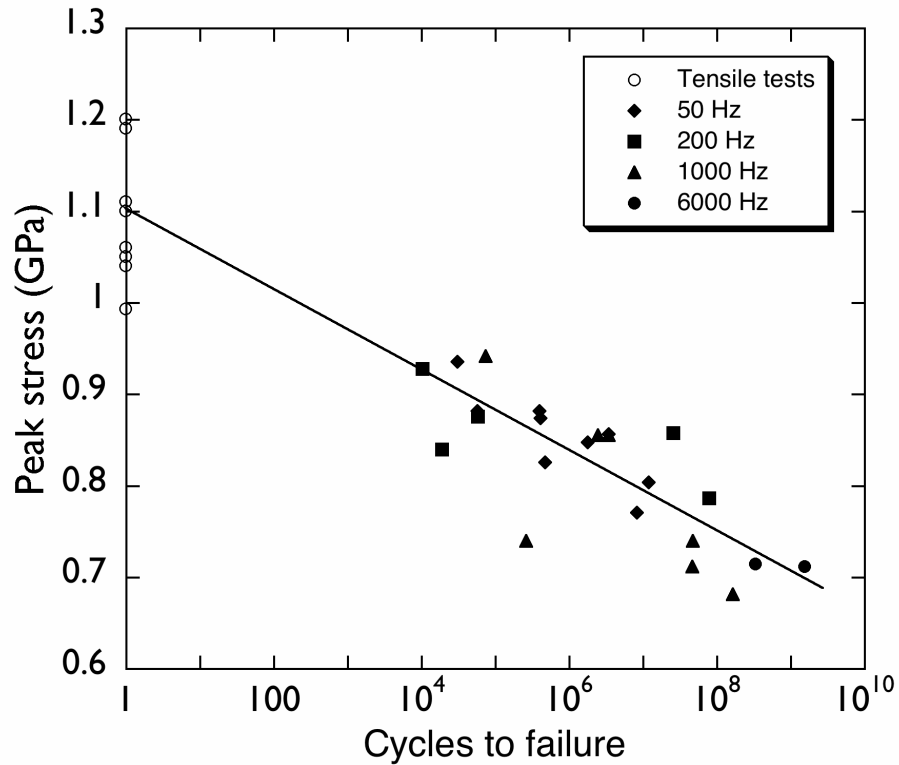
under cyclic loading. Although no measurements of the oxides were made, these surface topology changes were ascribed to the roughening of the surface oxide layer; this in turn was associated with a mechanism of cyclic stress-assisted dissolution of the oxide layer that could result in fatigue crack nucleation through the evolution of surface grooves.



**Figure 2.14:** Surface topography evolution showing in a series of AFM surface scans of the area below the notch root: (a) Before actuation, (b) After the actuation of polysilicon structures for  $2 \times 10^9$  cycles on a  $2 \mu\text{m} \times 2 \mu\text{m}$  scale; (c) and (d) are corresponding images on a  $5 \mu\text{m} \times 5 \mu\text{m}$  scale (before and after actuation, respectively), (e) Location of scan area at the vicinity of the notch root of the fatigue resonator (similar design as shown in Figure 2.2) corresponding to (a)–(d).[12]



**Figure 2.15:** Scanning electron microscope image of the miniature tensile specimen used in the study of Bagdahn and Sharpe [53-55]. The free paddle is attached to an external loading system during the fatigue test.



**Figure 2.16:** Stress-lifetime ( $S/N$ ) curve of thin-film polysilicon tensile specimens during cyclic loading tested with different loading frequencies between 50 and 6,000 Hz.[54]

The specific influence of frequency on the high-cycle fatigue behavior of thin-film polysilicon (3.5  $\mu\text{m}$  thick, 1.1 GPa tensile strength) was investigated by Bagdahn and Sharpe [53-55], who derived  $S$ - $N$  fatigue curves using tensile specimens (Figure 2.15) cycled at 50, 200, 1000 and 6000 Hz. Results showed similar trends at all frequencies (Figure 2.16); the fatigue life increased with decreasing maximum tensile stress, with specimens failing after  $10^9$  cycles at a peak stress of 0.7 GPa, some 35% lower than the tensile strength of the material (Figure 2.10). SEM images revealed probable failure initiation from the sidewalls, which was assumed to be caused by a defect generated under cyclic loading. AFM measurements of the surface roughness revealed that the surface near the fracture site was significantly rougher (17.2 nm) than the surface of a specimen not subjected to high cyclic stresses ( $\sim 8$  nm). The authors concluded that cracking induced by the environment only could not be the mechanism responsible for the fatigue behavior of silicon thin films, as a purely environmentally-assisted cracking mechanism would lead to a constant failure *time*, independent of the frequency [56]. Instead, their results suggested that the number of loading *cycles* to failure was independent of frequency, i.e., the time to failure decreased with increasing frequency. They concluded that most likely, an additional effect (other than the environmental influences) was present to account for these results.

Finally, additional  $S$ / $N$  data on 15  $\mu\text{m}$  thick polysilicon were recently published by Ferraris *et al.* [57], who used a comb-driven reciprocal rotor actuator, similar to the design used by White *et al.* [58], which causes a fully reversed bending load in an unnotched beam. They presented an  $S$ / $N$  fatigue curve where the stress is given on a relative scale, based on capacitive displacement measurements (Figure 2.10). They

observe delayed failure after  $\sim 10^9$  cycles for applied stresses of a  $\sim 70\%$  of the single cycle fracture stress. No failure was found for devices run for more than  $10^9$  cycles at stresses varying from 50 to 80% of the single cycle fracture stress. No mechanistic explanations were presented.

**Table 2.2:** Summary of fatigue testing of polycrystalline silicon thin films from 1999 to 2006. The upwards and downwards pointing arrow-symbols refer respectively to increases and decreases.

Authors	Specimen Geometry	Actuation Mode / Output Signal Measurement	Frequency $f$ , Stress Ratio $R$	Results
Van Arsdell, Brown [32]	Precracked cantilever beam (20 $\mu\text{m}$ wide, 40 $\mu\text{m}$ long, 2 $\mu\text{m}$ thick) attached to large plate.	Electrostatic actuation at resonance (in-plane motion). Capacitive sensing of motion.	45-48 kHz $R = -1$	$f_0 \downarrow$ during lifetime (wet air, $K_{app} = 0.3 \text{ MPa}\cdot\text{m}^{1/2}$ ). $f_0$ constant in dry air. $f_0$ constant with uncracked cantilever beam. Transgranular crack path.

## 2.4 Discussion of fatigue data and mechanisms

The results presented above clearly establish the phenomenon of the susceptibility of micron-scale single and polycrystalline silicon films to fatigue failure in ambient air under cyclic loading; this is in contrast to bulk silicon which shows no such susceptibility to cyclic fatigue. Based on a wide spectrum of studies (listed in Tables 2.1 and 2.2) involving a range of different testing methods (described in Appendix A), stress-lifetime data (Figures 2.1, 2.10) for thin-film silicon show relatively consistent trends (despite different test frequencies and load ratios), specifically that stress amplitudes as low as half the (single-cycle) fracture stress can cause delayed fatigue failure, typically after  $10^{11}$  cycles or more [11,24,31,33]. Such fatigue failure has been reported for various modes of cyclic loading, specifically for fully reversed cyclic loading ( $R = -1$ ) [4,11-15,18,19,24,30-35,41-43,50-52,57] and tensile loading with a positive mean stress ( $R \geq 0$ ) [13,21-23,25-29,33-35,40,53-55]. More importantly, the frequency of loading does not appear to influence the fatigue life [26,27,53-55]. These results suggest that the mechanism(s) responsible for such thin-film silicon fatigue must include both time-independent and cycle-dependent contributions, and that the phenomenon is unlikely to be the sole result of environmentally-induced cracking [28,29,34], as this would lead to lifetimes in terms of time (and not in terms of cycles) which are frequency-independent [56].

In terms of physical understanding, two classes of mechanisms have been proposed to explain the fatigue degradation of silicon films. As noted above, the first of these associates the fatigue degradation process with a surface phenomenon. The most prominent mechanism of this type is the reaction-layer fatigue mechanism (Figure 2.12)



[11,42], which attributes thin-film silicon fatigue to a process of sequential, cyclic stress-induced oxidation and moisture-assisted cracking of the surface silicon-oxide layer. In this mechanism, subcritical crack growth occurs solely in the amorphous silicon oxide layer, and is associated with the well-known processes whereby the hydroxyl ions in water react chemically with the  $\text{SiO}_2$  at the crack tip to destroy the polar siloxane bonds and replace them with weaker hydrogen bonds [59]. Such environmentally-assisted cracking in the oxide leads to failure of the entire structure when the critical crack size is exceeded. The second class of mechanisms asserts that the damage processes evolve from purely mechanical subcritical cracking in the silicon itself [13].

On the basis of the evidence presented in the studies reviewed, the reaction-layer mechanism appears to account for most experimentally observed effects. First and foremost, the absence of delayed thin-film silicon fatigue failures in low-grade vacuum, and the observed influence of humidity on the fatigue life are strong indications of a significant environmental contribution to cracking (Figure 5) [19,20,30,31]. However, observations that the number of cycles to failure is frequency-independent are clear indications of a true fatigue contribution too (Figure 2.16) [26,27,53]. Indeed, cyclic effects associated with moisture-assisted cracking of the silica layer are very plausible. Although it is a common belief that cyclic loading does not accelerate crack-growth rates in silicon-oxide structures [56], cyclic fatigue has been reported for a borosilicate glass at very low growth rates ( $< 3 \times 10^{-8}$  m/s) [60]. In addition, stress-life fatigue curves generated for nano-scale silicon oxide beams did not exhibit a dependence on frequency [26,61], again suggesting pure cyclic effects. Second, as noted above, the fact that macro-scale silicon does not display fatigue susceptibility is consistent with the lack of influence

of cracks in the silica layer at these larger scales. In macro-scale structures, critical crack sizes to cause unstable fracture cannot be reached by cracks inside the oxide layer (which naturally does not scale with the size of the structure). Finally, the weakening effect, induced at compressive mean stresses and high fatigue amplitudes, as well as at low tensile mean stress and high fatigue stress (Figure 2.9) [13] can also be explained. All these test conditions introduce fatigue damage by cyclic loading, lowering the apparent strengths. However, the reported strengthening at low stress amplitudes, where the mean stress is highly compressive or highly tensile [13], cannot be explained by any mechanism at present and remains somewhat of a mystery.

The precise origin of the cyclic stress-assisted oxidation of silicon, which plays an important role in the reaction-layer fatigue mechanism, is not known. However, it is likely related to some form of stress-assisted diffusion or an increased oxidation reaction rate at the silicon/oxide interface. Compressive stresses occur in the silicon-oxide layer during oxidization because the molar volume of  $\text{SiO}_2$  ( $27 \text{ cm}^3/\text{mol}$ ) is larger than for Si ( $12 \text{ cm}^3/\text{mol}$ ). The decrease in oxidation rate as the silicon-oxide layer grows has been partly attributed to the presence of these stresses, because of a decrease in oxidant diffusion rate [62-64]. Additionally, tensile stresses in the silicon generated by the oxide can cause the oxidation reaction at the silicon/oxide interface to occur more quickly [65]. When applying a cyclic load, the compressive stresses in the silicon oxide will be relieved during the tensile part of the loading cycle, which results in a smaller decrease in the oxidation reaction rate as the oxide grows thicker. Moreover, in combination with an applied compressive load in another part of the loading cycle, which increases the oxidation reaction, a rapid oxidation process could occur that results into the growth of a

thicker oxide. This oxide thickening effect has been observed in all the fatigue studies where oxide thicknesses have been measured (Figure 11 [11]), and is one clear characteristic of micron-scale silicon fatigue. With the direct observations of subcritical cracks in these oxide layers (Figure 11) [11,42], which is shown to be consistent with the coupling of damage accumulation and decrease in resonance frequency of fatigue specimens (Figure 13) [11], as well as surface roughening at points of high stress (Figure 16) [12,54] as a result of the oxidation process, there is a compelling list of experimental evidence to support the reaction-layer mechanism. In contrast, this experimental evidence is lacking for mechanisms based on subcritical cracking of the silicon itself, as was shown in section 3.

Since silicon is neither prone to environmentally-assisted cracking nor fatigue failure in bulk form, these latter mechanisms of thin-film silicon fatigue involving subcritical cracking in the silicon itself are in essence totally inconsistent with the vast majority of experimental evidence. Therefore mechanisms based on subcritical cracking in the oxide layer provide the only realistic explanation for the fatigue of silicon at the micron-scale. The experiments that will be presented in the next chapter, will answer the question what the effect of a high humidity environment as well as a high vacuum environment is on the stress-lifetime behavior of polysilicon. Furthermore, the influence of the initial silicon oxide thickness on the stress-lifetime fatigue behavior will be investigated. The results of these experiments will lead to the conclusive proposition of a mechanism for fatigue in micron-scale silicon.

## 2.5 Summary and conclusions

Silicon is widely used in microelectromechanical systems applications. However, because of its brittle nature, it is clearly not an ideal structural material. Although bulk silicon is not susceptible to fatigue, micron-scale silicon displays delayed failures under cyclic fatigue loading at applied cyclic stresses as low as half the (single-cycle) fracture strength. Since the early 1990s, several mechanisms to explain such fatigue failures in micron-scale silicon (both single and polycrystalline) have been suggested. These mechanisms can be divided into two main classes, namely those that attribute fatigue to a surface effect caused by cracking in the silicon-oxide layer (e.g., reaction-layer fatigue) and those that propose subcritical cracking in silicon as the cause of thin-film silicon fatigue.

Based on a review of the extensive literature on this topic, it is apparent that in general the stress-lifetime (S/N) fatigue data that have been measured by numerous authors all display similar trends, wherein lower cyclic stresses lead to a larger number of cycles to failure. Lifetimes are found to depend markedly on the environment, but not on loading frequency when considered in terms of cycles (and not time) to failure. It is argued that the published data from fatigue studies in both single and poly crystalline silicon present no convincing evidence to support the notion that the salient fatigue mechanisms involve subcritical cracking in the silicon itself. On the contrary, the vast majority of experimental evidence on micron-scale, thin-film silicon fatigue is consistent with the concept of a reaction-layer fatigue mechanism, where delayed failures result from cyclic stress-induced oxidation and consequent moisture-induced subcritical

cracking in the silicon-oxide surface layer. Additional fatigue experiments presented in the next section will conclusively show this.

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## Chapter 3

# Fatigue in micron-scale polycrystalline silicon structural films

### 3.1 Introduction

Silicon is the most widely used material for microelectromechanical systems (MEMS) sensors and actuators, as was illustrated in Chapter 1. This is largely a result of the ease with which silicon can be microfabricated to produce complex mechanical structures in thin film form, because of highly developed processing methods directly related to semiconductor electronics processing [1,2]. However, as was also illustrated earlier, silicon is not an ideal structural material; it is quite brittle and subject to several reliability concerns – most importantly, stiction [3,4], wear [3,5] and fatigue [6-24] – that strongly limit the utility of silicon MEMS devices in commercial and defense applications. In particular, premature fatigue failure can occur when devices are subjected to a large number ( $\sim 10^6$  to  $10^{12}$ ) of loading cycles at stress amplitudes well below their monotonic fracture stress; this may arise from vibrations intentionally induced in the structure (e.g., resonators found in radio frequency MEMS applications) or due to the service environment (e.g., engine vibration on a airbag deployment accelerometer in a car). Additionally, because the surface-to-volume ratio in these structural films is very large, traditional failure models that have been developed for materials at the bulk scale

cannot always be relied upon to accurately predict behavior, essentially because new physical mechanisms may be operative. Indeed, it is clear that at these length scales, surface effects may become dominant in controlling mechanical properties. While the reliability of MEMS has received extensive attention, the mechanisms responsible for the various failure modes have yet to be conclusively determined. This is particularly true for the fatigue of micron-scale silicon films, a research area that has been the subject of intense debate [6-24], as was discussed in Chapter 2.

Although bulk silicon is not susceptible to fatigue failure in ambient air [25,26], thin silicon structural films are [6]. In Chapter 2 it was proposed that the fatigue of micron-scale polycrystalline silicon (polysilicon) films is a result of a reaction-layer fatigue process [10-12], whereby high local cyclic stresses induce thickening of the post-release amorphous  $\text{SiO}_2$  oxide layer at stress concentrations such as notches. As silica is highly sensitive to environmentally-assisted fracture, subcritical (stable) cracking induced by the presence of moisture occurs within the oxide layer to form a crack large enough to fracture the entire device. The mechanism explains why bulk silicon is not susceptible to such fatigue failure as subcritical cracks within the oxide layer can never get large enough to cause fracture of the entire structure.

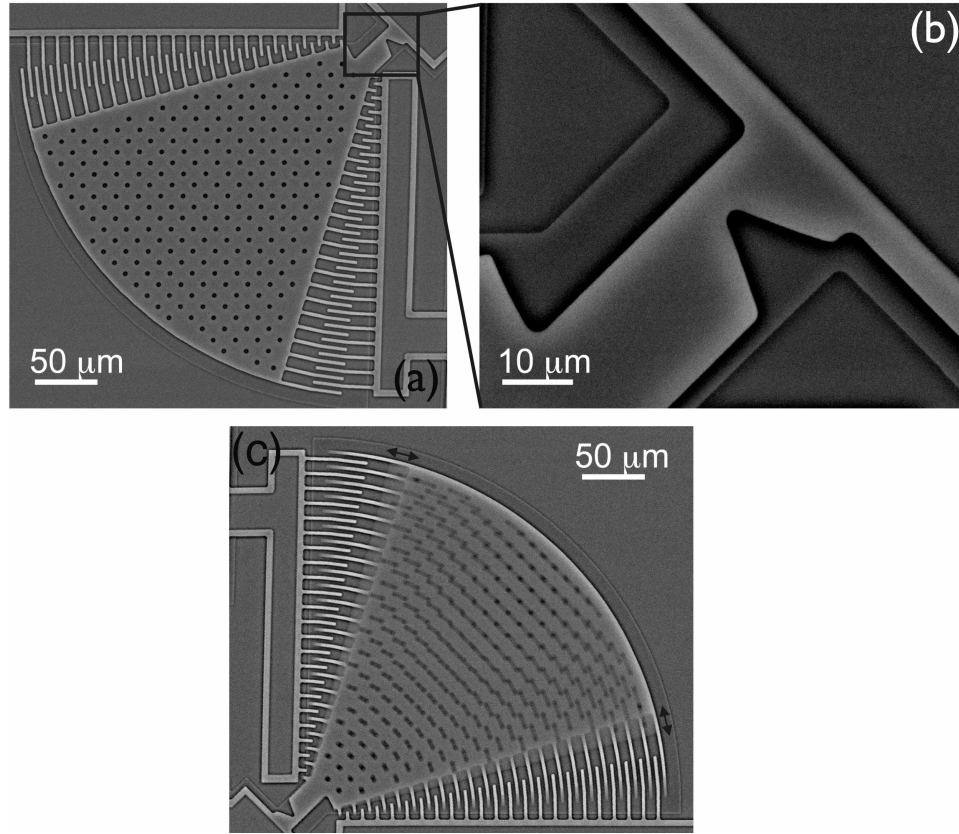
As also was shown in Chapter 2, the reaction-layer fatigue mechanism has been called into question by some researchers [14-16] who instead proposed a series of alternative mechanisms, all of which are purported to account for the fatigue effect occurring in (polycrystalline) silicon. In these counter arguments, fatigue damage is suggested to be strongly affected by the compressive portion of the loading cycle, with (i) crack growth due to a mechanism similar to cyclic compression fatigue of notched, brittle

ceramic bulk specimens [27] aided by a wedging effect of silicon debris or the oxidized surface inside the crack, or (ii) that crack growth occurs by dislocation activity, which causes either crack-tip blunting, or crack-tip blunting followed by sharpening (similar to fatigue in ductile materials), or (iii) that grain-boundary deformation by means of shear deformation in the thin amorphous region of a grain boundary hitting the surface causes stable crack growth. All these suggested mechanisms suffer from the fact that they cannot explain why micron-scale silicon is susceptible to fatigue and bulk silicon is not; more importantly, no direct experimental evidence to support these proposed alternative mechanisms is given. Indeed, crack growth in compression associated with debris or surface oxidation induced “cantilever effects” have been largely discounted as a mechanism of tensile fatigue in brittle materials; Pierron and Muhlstein [28] have further shown that such phenomena will not cause an increase in the magnitude of the stress intensity factor at the crack tip. Additionally, our detailed observations have revealed no evidence for asperity contact, dislocation activity under these particular loading conditions, nor of grain-boundary plasticity; similarly, there have been no reports to our knowledge in the literature of such phenomena. Moreover, since single crystal silicon also displays similar fatigue behavior [6,8,29,30], universal mechanisms involving grain boundaries are unlikely to be too relevant. The purely mechanical alternative mechanisms ignore the role of stress-induced oxide thickening, which has been observed now by several investigators [11,18,22]; further, this brings into question whether the polysilicon films utilized in these studies were representative due to their relatively thick post-release oxide scales (typically ~20-30 nm [11] rather than the order of a magnitude smaller native oxide layers expected for polysilicon [31]). Pierron *et al.* [32], however, have

recently shown that the relatively thick post-release oxide layers found in these devices, which were all fabricated in the Multi User MEMS Process (MUMPs) foundry [33,34], arise from a galvanic effect of the n+-type silicon and gold in concentrated HF during release of the free-standing structures at the end of the fabrication process, a finding that was later confirmed [35].

In these experiments, *on-chip* MEMS testing chips and a series of transmission electron microscopy (TEM) techniques are used to further investigate fatigue in micron-scale n-type polysilicon MEMS resonators. In light of the discussion [6-24] outlined in Chapter 2 concerning the mechanism of such thin-film silicon fatigue, the prime objective of this study is to examine the susceptibility to fatigue of polycrystalline silicon films with much thinner initial oxide layers, specifically fabricated by the Sandia SUMMiT<sup>TM</sup> process, and to verify the reproducibility of previous findings across fabrication runs with respect to fatigue properties and oxide-layer thicknesses. Additionally, the changes in fatigue behavior and the development of reaction layers with environment was characterized, in both relatively oxygen-/moisture-free and moisture-rich, high relative-humidity environments. Also specifically examined was the fatigue susceptibility of polysilicon films with thin initial oxide layers *in vacuo*, where resistance to fatigue would be expected to be the largest.

### 3.2 Experimental procedures



**Figure 3.1:** Scanning electron micrographs of the polysilicon MEMS fatigue life characterization resonator. (a) Triangular free standing proof mass with interdigitated comb drive on one side and capacitive displacement sensor combs on the other side; (b) notched cantilever beam ( $\sim 40\text{ }\mu\text{m}$  long,  $\sim 19.5\text{ }\mu\text{m}$  wide with a  $\sim 13\text{ }\mu\text{m}$  deep,  $\sim 1\text{-}0.3\text{ }\mu\text{m}$  root radius notch) connecting the resonator mass to the anchor; (c) resonator device operated *in situ* in a scanning electron microscope – in the image the edges of the comb fingers are blurred because of the high frequency motion.

Low pressure chemical vapor deposited (LPCVD) phosphorous-doped polysilicon fatigue resonator devices from both the MUMPs foundry (fabrication runs 18 and 50) [33,34] as well as the Sandia National Laboratories SUMMIT<sup>TM</sup> process [36] were studied. Both set of devices, i.e., *on-chip* fatigue specimens, were fabricated using the

same device design originally developed by Van Arsdell *et al.* [37]. The device consists of a  $\sim 300 \mu\text{m}$  sized triangularly shaped free-standing proof mass connected to an anchor on the substrate by a notched cantilever beam (see Figure 3.1). The mass is electrostatically driven at resonance in plane with fully reversed loading ( $R = -1$ , where  $R$  is the ratio of minimum to maximum stress) by an interdigitated comb drive at one side of the device, whereas the comb-structure on the other side of the proof mass is used to capacitively sense the displacement of the device during operation. Using the measured (calibrated) displacement and finite-element calculation based on linear elasticity methods (ANSYS 5.7) the stress at the notch in the cantilever beam during the test can be readily calculated. More details on these finite element calculations can be found in [9].

The electrostatic actuation is based on applying a bias across the set of combs in the comb drive. The magnitude of the force created by the drive is given by:

$$F = \epsilon \frac{nh}{g} V^2 \quad (3.1)$$

where  $\epsilon$  is the dielectric constant of the medium between the comb finger,  $n$  is the number of comb finger,  $h$  the thickness of the comb fingers,  $g$  the gap between the fingers and  $V$  the applied voltage [38]. When a sinusoidal voltage ( $V = A_0 \sin \omega t$ ) is applied to the comb drive, it can be shown that the magnitude of the resulting force ( $F$ ) is proportional to  $A_0^2 \cos 2\omega t$ . Consequently, by applying a sinusoidal voltage at half the resonance frequency, the device can be run at resonance. Capacitive displacement sensing is done by measuring a small current flowing from the opposite set of combs that originates by changing the capacitance of the set of overlapping comb fingers while applying a constant DC voltage. Custom-built electronics, which also filter this signal using an adjustable band-pass filter, convert the current into a voltage that is led into a computer

system running LabVIEW. After optically calibrating this voltage with the corresponding displacement, measuring the displacement as function of the driving frequency allows the fatigue resonator devices to be run at resonance. The resonance frequency and the displacement can be periodically updated during the test by sweeping the frequency and monitoring the displacement. This feedback mechanism allows the displacement to be held constant during the test. Finite-element modeling has shown that a decay in the resonance frequency of the resonators during the test can indicate both cracking, as well as oxide formation, at the notched cantilever beam [11].

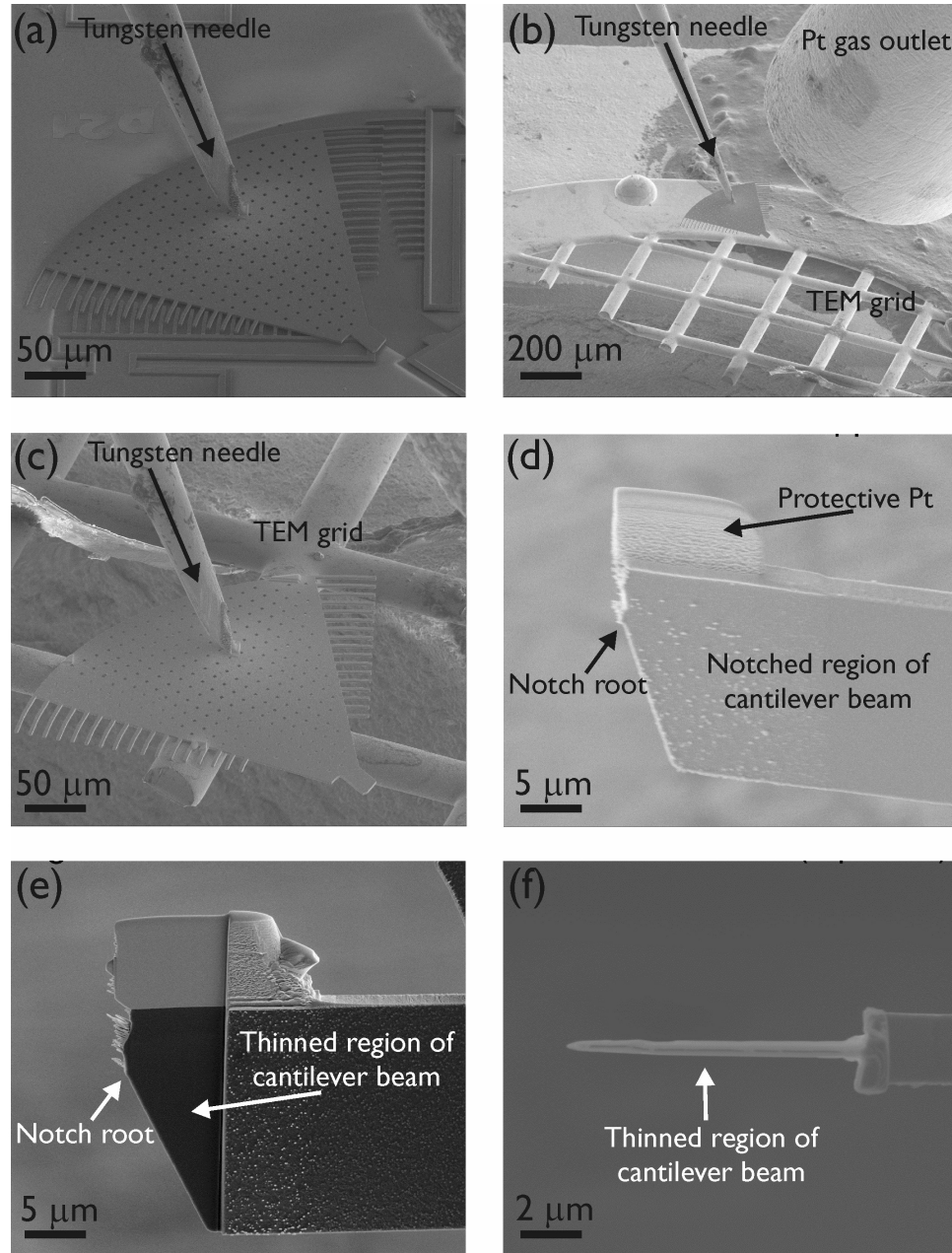
The n+-type polysilicon (resistivity  $\rho = 1.9 \times 10^{-3} \Omega\cdot\text{cm}$  [33];  $\sim 10^{19}$  atoms/cm<sup>3</sup> phosphorous [9]) MUMPs devices were fabricated in run 50 of the process and had a structural film thickness of 2  $\mu\text{m}$  and a resonance frequency of approximately 40 kHz. To calibrate the capacitive displacement sensing, this type of device was run in a microvision system [9,18] and *in situ* under a regular optical microscope. The SUMMiT<sup>TM</sup> devices came from the five-layer polysilicon process and were n-type polysilicon with structural film thicknesses of 2.25  $\mu\text{m}$  for devices fabricated from layer P3 and 2.5  $\mu\text{m}$  for devices from a stack of layers P1 and P2 (P21). Resonant frequencies are approximately 36 kHz and 37 kHz respectively and calibration of these devices was performed *in situ* under an optical microscope. All devices are packaged in dual inline packages and ultrasonically bonded aluminum wires are used to connect the package wiring to the contact pads on the MEMS chips.

Using the system described above, experiments were performed in ambient air (25 °C, 30-40% relative humidity (%RH)) for both type of devices and both film thicknesses to determine applied stress vs. total life (*S/N*) curves. High relative-humidity air



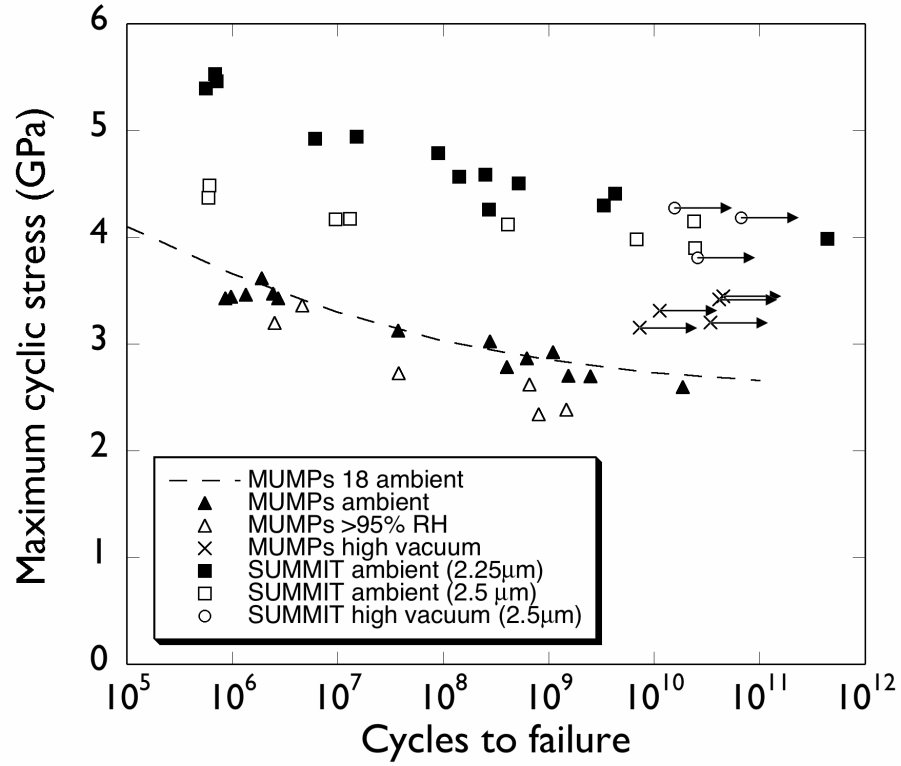
experiments ( $\sim 25^\circ\text{C}$ ,  $>95\% \text{RH}$ ) were performed on the MUMPs devices in an environmental chamber by bubbling dry air through two water vessels. Both the MUMPs devices as well as the SUMMiT<sup>TM</sup> devices have been run in very high vacuum ( $\sim 25^\circ\text{C}$ ,  $<2.0 \times 10^{-7}$  mbar), although for the SUMMiT<sup>TM</sup> devices only the P21 devices were operated *in vacuo*.

Following fatigue testing, the fatigued and fractured beams were imaged using TEM. The MUMPs resonator proof masses were transferred to copper TEM clamshell grids and observed in the unthinned condition in the Berkeley JEOL-JEM 1000 high-voltage transmission electron microscope (HVTEM) operated at 800 keV. After thinning using a dual-beam focused-ion beam (FIB) system (FEI Strata DB235 Dual Beam FIB), the SUMMiT<sup>TM</sup> devices were imaged in a Philips CM200-FEG, operated at 200 keV, with a Gatan Image Filter (GIF) system; this allows energy-filtered imaging to create an elemental map of an area of interest (so-called energy-filtered transmission electron microscopy, or EFTEM). Inside the FIB, a sharp tungsten micromanipulator needle was used to move the fractured resonator masses from the MEMS chip surface to (half) a copper TEM grid by temporarily welding it to the resonator mass with deposited platinum (Figures 3.2(a)-3.2(c)). A  $\sim 100$  nm thick carbon layer was sputtered onto some of the samples to assure that the oxide layers would be delineated more clearly. Using standard FIB techniques [39], the area at the notch was thinned starting from the side of the ligament not containing the notch, after depositing a protective layer of platinum on the same side (Figures 3.2(d)-3.2(f)). Applying the platinum layer, as well as ion milling from the back of the sample, was necessary to prevent ion implantation during thinning and subsequent damage of the surface.



**Figure 3.2:** FIB thinning TEM sample preparation method for SUMMiT™ devices. (a) tungsten micro-manipulator needle is welded to the fatigued resonator and is lifted above the substrate; (b) resonator is moved over to the TEM grid; (c) resonator is Pt welded to the TEM grid; (d) after removing the needle from the resonator a protective layer of platinum is deposited (some of the samples also had a carbon layer sputtered on top to make the oxides stand out more clearly); (e),(f) electron transparent thinned sample. The thinned region of the beam in (e) is perpendicular to the plane of the image in (f).

### 3.3 Stress-lifetime fatigue

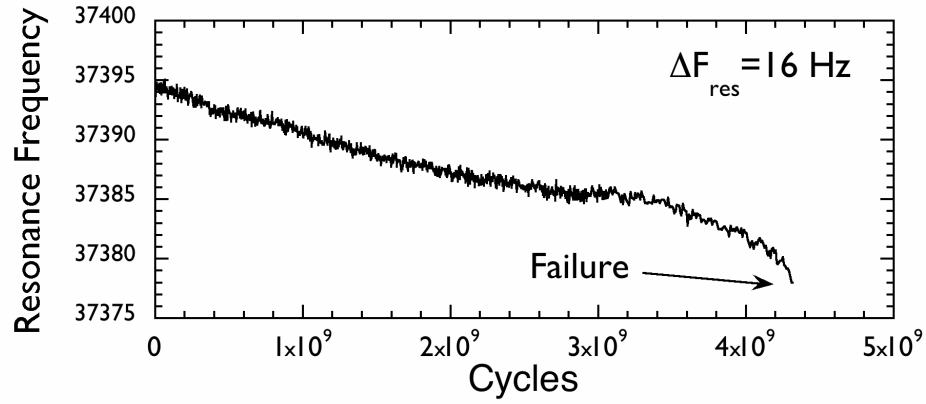


**Figure 3.3:** Combined maximum cyclic stress lifetime ( $S/N$ ) data (at  $R = 1$ ) for polysilicon MUMPs and SUMMIT<sup>TM</sup> devices, the last type with two different structural silicon film thicknesses (2.25  $\mu\text{m}$  and 2.5  $\mu\text{m}$ ). Different types of devices are tested in ambient air ( $\sim 25^\circ\text{C}$ , 30-40 %RH), high relative humidity ( $\sim 25^\circ\text{C}$ , >95 %RH) and very high vacuum ( $\sim 25^\circ\text{C}$ ,  $< 2.0 \times 10^{-7}$  mbar). For comparison, a curve fit to fatigue data from MUMPs run 18 by Muhlstein *et al.* [10,11] is also shown.

Figure 3.3 shows a comparison of the maximum applied cyclic fatigue stress-lifetime ( $S/N$ ) data for both the MUMPs (run 50) and SUMMIT<sup>TM</sup> devices, tested in air, high humidity and high vacuum, with previous air data for MUMPs devices (run 18) from [11]. Several trends are apparent in these results, which run out to lifetimes approaching  $10^{12}$  cycles, i.e., on the order of 10 months.

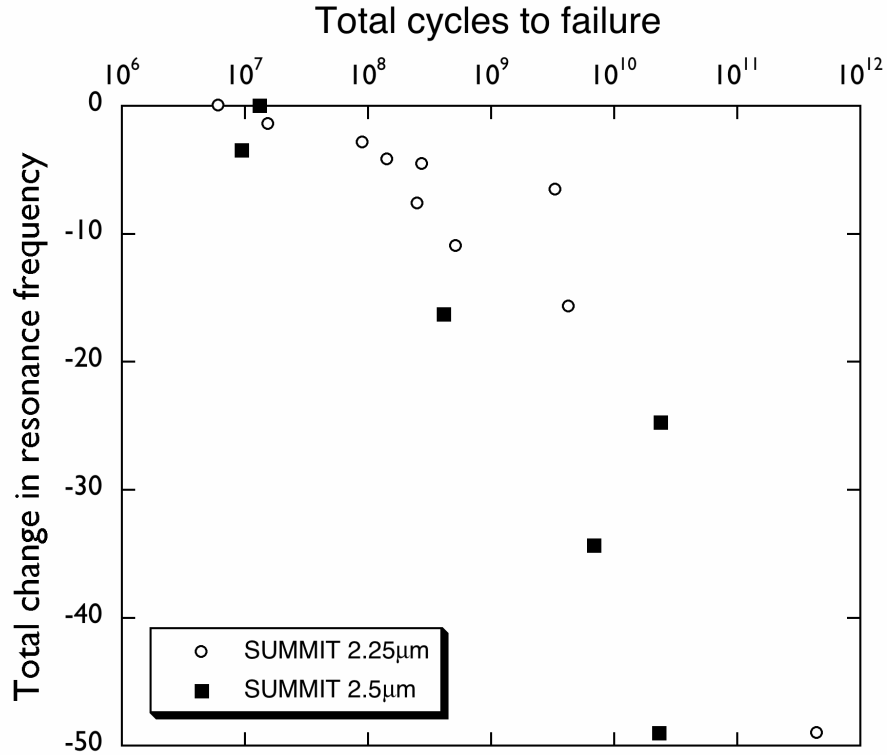
1. All curves for tests in air (~25 °C, 30-40 %RH) show typical *S/N* type behavior with lower applied stresses resulting in a larger number of cycles to failure (Figure 3.3). Specifically, at stresses of ~70% of the fracture stress, failures occur after some  $10^{11}$  cycles. Close correspondence is seen between the two sets of MUMPs devices, from the earlier fabrication run 18 [10,11] to the current run 50; compared to the SUMMiT™ runs, these devices have lower fatigue resistance.
2. The extent of accumulated fatigue damage, which can be primarily associated with oxidation and crack growth and is confirmed by finite-element modeling [40], was qualified for the SUMMiT™ samples by monitoring the change in resonance frequency throughout the fatigue tests (Figure 3.4). For all tests in air, a monotonic decrease in resonance frequency was observed during the entire fatigue life up until the point of failure, similar to that reported previously for the fatigue of the MUMPs devices [11]. A larger total decrease in resonance frequency at the point of failure was found for tests run at lower stress, as shown in Figure 3.5. The relation between the number of cycles to failure and total decrease in resonance frequency can be qualitatively compared to the proportionality following from the expression for the stress intensity:  $K \propto \sigma\sqrt{a}$ , where  $\sigma$  is the stress and  $a$  the crack length. Plotting the number of cycles to failure exponentially ( $\propto$  to the applied cyclic stress  $\sigma$ , as can be derived from the experimental *S/N* results in Figure 3.3) versus the change in resonance frequency ( $\propto$  to the crack length  $a$ , here assumed to be roughly the same size as the thickness of the oxide layer), a (negative) second-order trend can be found (Figure 3.5). This also shows that the experimental, yet indirect, crack-propagation measurements by monitoring the resonance frequency are consistent with the

theoretical expression for the stress intensity reached at failure and therefore give a good indication of damage accumulation in these test samples.



**Figure 3.4:** Typical example of resonance frequency ( $F_{res}$ ) behavior of SUMMiT™ devices during fatigue tests. The decrease in resonance frequency ( $\Delta F_{res}$ ) with number of cycles throughout the fatigue life is associated with damage accumulation, in the form of oxide growth and subcritical cracking within the oxide layer.

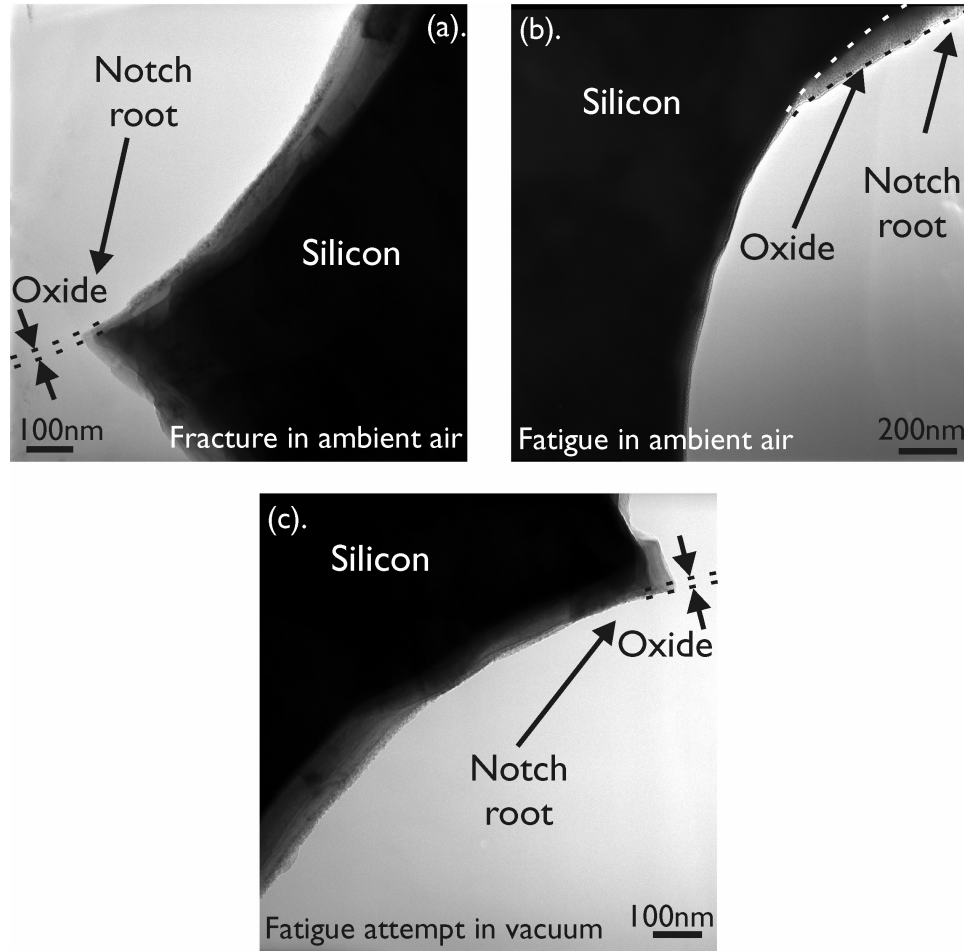
3. Increasing the relative humidity to greater than 95% for MUMPs devices was seen to lower the fatigue lifetimes at a given stress compared to behavior in ambient (30-50 %RH) air. Although scatter in the fatigue results and the logarithmic nature of the  $S/N$  plot tend to mask the effect somewhat, all data points for fatigue tests run in the 95% relative humidity environment lie on a different  $S/N$  curve below the curve acquired in ambient air (Figure 3.3). A grouped linear regression and analysis of covariance has shown that the slopes of the two sets of data have a 28% similarity, whereas the line separation shows that they the two sets of data only have a 0.02% similarity. This distinctly shows that the two data sets are different.



**Figure 3.5:** The total resonance frequency decay at the point of failure for the two types of SUMMIT<sup>TM</sup> devices (2.25 and 2.5  $\mu\text{m}$  silicon structural device layer thickness) plotted versus the total number of cycles to failure. A (negative) second-order exponential trend can be observed between the total frequency decay and the number of cycles to failure.

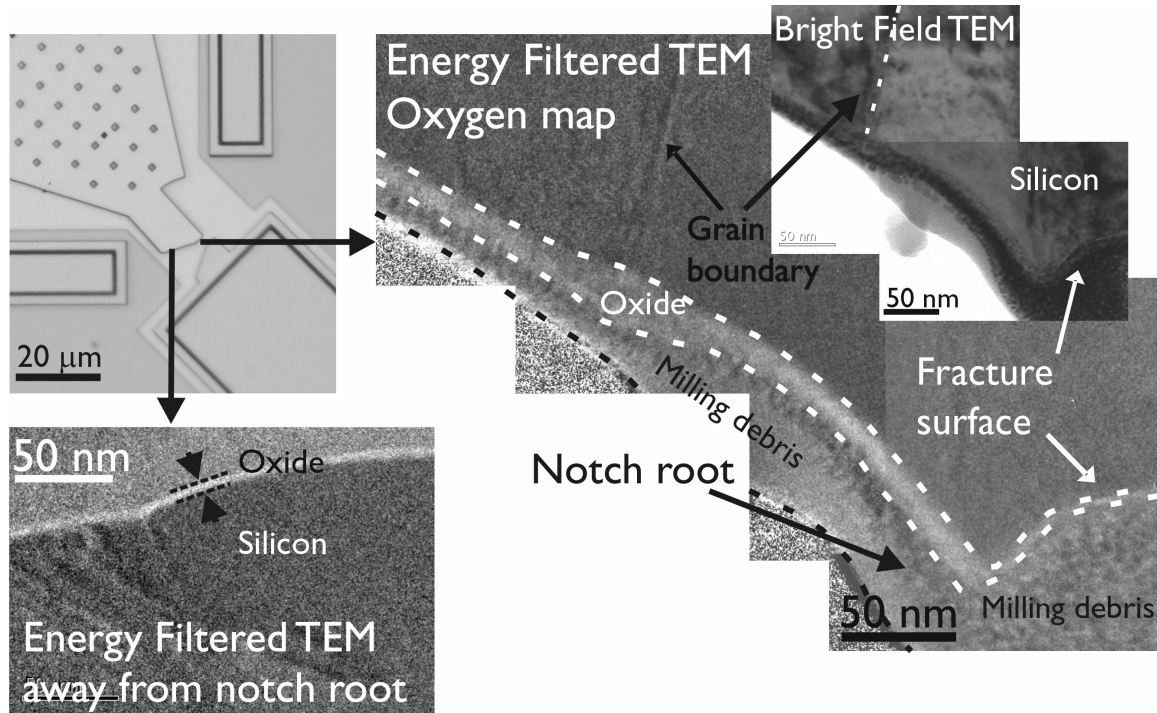
4. No fatigue failures occurred under very high vacuum conditions ( $\sim 25^\circ\text{C}$ ,  $< 2.0 \times 10^{-7}$  mbar). All the samples tested *in vacuo* survived some  $10^9$ - $10^{10}$  cycles at high stresses without failure (in Figure 3.3, these data points are plotted as run-outs, i.e., at the point where testing was stopped without failure). Moreover, no progressive fatigue damage accumulation or oxidation could be detected throughout these tests, as indicated by the lack of change in natural frequency of the device; this is in stark contrast to fatigue tests in air, where there was a continuous and progressive decay in the resonant throughout the life.

### 3.4 Oxide layers characterization



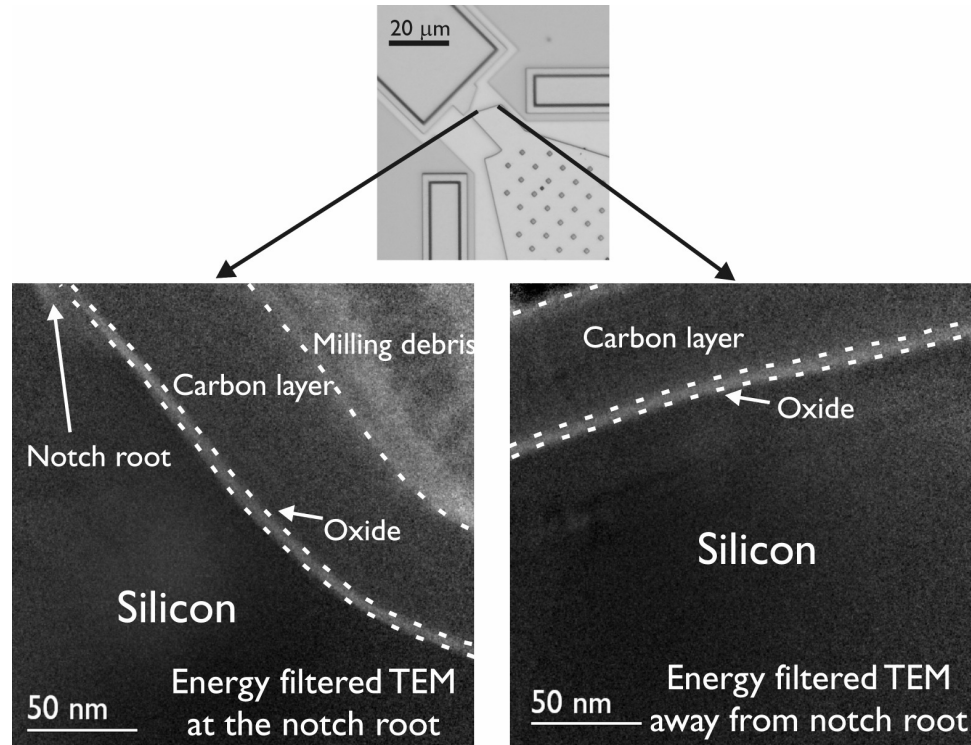
**Figure 3.6:** HVTEM images from failed MUMPs resonator devices. (a) Monotonically fractured specimen in ambient air; no (local) oxide thickening. At the edge of the sample some contrast in grains is visible (because of sample tilt); however, only the outer region of the edge is amorphous. (b) Fatigued in ambient air with thickened oxide layer at the notch root (maximum cyclic stress at the notch root: 2.86 GPa; number of cycles at failure:  $6.28 \times 10^8$ ). (c) Device after fatigue attempt *in vacuo* and subsequent single-cycle fracture; no oxide layer thickening (maximum cyclic stress at the notch root during fatigue attempt: 3.29 GPa, number of cycles when stopped:  $1.14 \times 10^{10}$ ). Also in this case contrast from grains on the edge is visible.

For the MUMPs devices, HVTEM imaging of unthinned fatigue specimens revealed a local thickening of the oxide layer at the notch root; for specimens fatigued in ambient air, oxide layers as thick as 100 nm were measured (Figure 3.6(b)). Such local notch-root oxide thickening was not observed for mechanically fractured (non-fatigued) specimens in ambient air (Figure 3.6(a)) nor for specimens fatigue cycled for up to  $10^{10}$  cycles *in vacuo* (Figure 3.6(c)). In these latter two cases, the post-release oxides were found to be ~15 - 30 nm thick, which is typical for the initial oxide thicknesses of MUMPs devices [32,35].



**Figure 3.7:** Energy-filter transmission electron microscopy (EFTEM) images (20 eV window around 532 eV oxygen edge) of surface oxides following fatigue failure in ambient air of a SUMMiT<sup>TM</sup> device, showing a thickened oxide around the notch root (15 nm) after fatigue up to 20 nm at a grain boundary terminating at the surface. Oxide layers of 3-5 nm have been observed away from the notch as well as on the freshly created fracture surface.





**Figure 3.8:** EFTEM images (20 eV window around 532 eV oxygen edge) of surface oxides of the surface oxide after fatigue cycling a SUMMiT™ device in very high vacuum ( $P < 2.0 \times 10^{-7}$  mbar), showing no local oxide thickening at the notch (left) in comparison with the oxide thickness away from the notch root of the same device (right). The oxide thickness for this device, which had a film thickness of 2.5  $\mu\text{m}$  in both stressed and unstressed regions, was 5-6 nm. It was cycled for  $6.7 \times 10^{10}$  cycles at a maximum cyclic stress of 4.14 GPa, without fatigue failure.

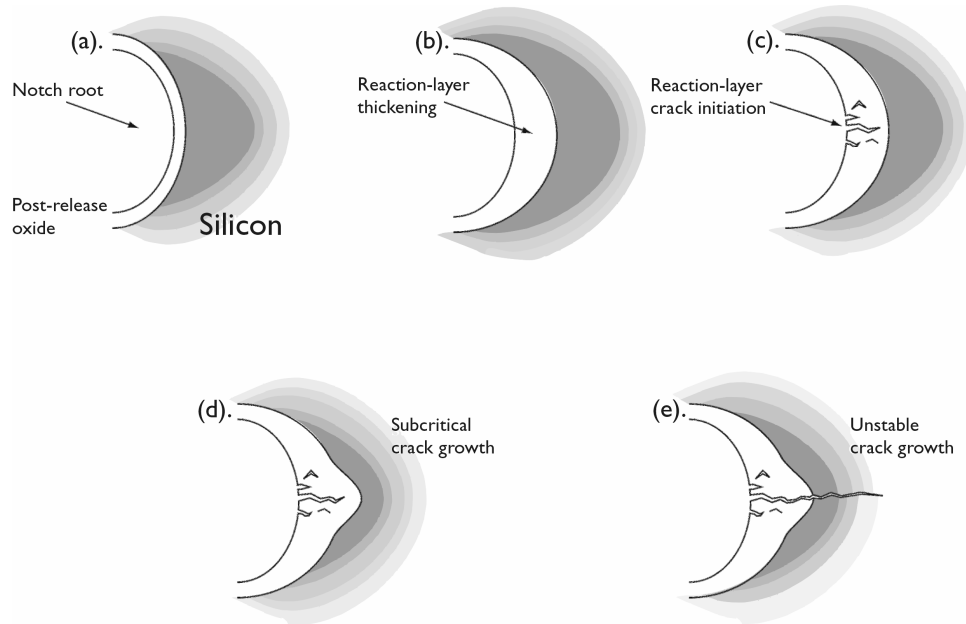
The SUMMiT™ devices have been processed to circumvent the galvanic effect associated with back-end-of-line metallization layers and consequently have a thinner post-release oxide than the MUMPs devices [32]. For the SUMMiT™ devices, EFTEM oxygen maps of FIB samples revealed a similar trend in oxide thicknesses, although the overall magnitude of these layer thicknesses was much smaller than for the MUMPs devices. The initial oxide layer thickness away from the notch root and on freshly created

fracture surfaces was between 3-6 nm in the SUMMiT™ devices, and was locally thickened at the notch root up to about 15 nm after fatigue failure (Figure 3.7). Interestingly, the oxide layer in locations where grain boundaries terminated at the surface did appear thicker up to ~20 nm (Figure 3.7(a)); this could be due to higher local stresses associated with the geometry of the grain boundary in such locations, or to faster oxidation rates at such sites of higher internal energy. In contrast, no oxide thickening was observed for devices cycled *in vacuo* (Figure 3.8), i.e., in the absence of moisture and oxygen, consistent with the device resonance frequency measurements (described above) which showed no evidence of accumulated damage during these tests.

### 3.5 Reaction-layer fatigue mechanism

The phenomenon of the time/cycle-delayed fatigue failure of micron-scale structural silicon films, an effect not seen in bulk silicon, is clearly an important failure mechanism that could limit the useful life of MEMS devices. In terms of traditional fatigue-crack growth mechanisms, which involve cyclic (e.g., dislocation) plasticity in ductile materials and a suppression of crack-tip (wake) shielding (e.g., crack bridging) in brittle materials [25], the notion that a prototypical brittle material such as silicon fatigues at all is at first sight a mystery. It was proposed, however, that such very high-cycle, thin-film silicon fatigue is associated with a reaction-layer fatigue mechanism [10-11] (Figure 3.9), where the actual fracture processes occur not in the silicon itself but by moisture-induced cracking in the cyclic stress-assisted thickened oxide layer. Stress/moisture-assisted cracking of the oxide layer, where hydroxyl ions in water react chemically with the SiO<sub>2</sub>, destroying siloxane bonds [41], induces stable crack growth

which, provided the oxide layer is thick enough, results in a crack inside this layer large enough to exceed the critical crack size for the entire structure, whereupon the structure fails catastrophically. Both oxide thickening during cyclic fatigue loading and the presence of nanoscale stable cracks within the oxide layer of these films after cycling have been directly observed [10,11]. Similarly, Allameh *et al.* [18] report a surface roughening effect at stress concentrations during fatigue of micro-scale silicon (also reported by Bagdahn and Sharpe [22]), and have suggested a complementary mechanism involving stress-assisted oxide thickening, caused by dissolution of the surface oxide, which forms deep grooves in the vicinity of the notch that become sites for crack initiation.



**Figure 3.9:** Schematic of the reaction-layer fatigue mechanism at the notch of the polycrystalline silicon cantilever beam (a),(b): Localized oxide thickening at the notch root. (c): Environmentally-assisted crack initiation in the native oxide at the notch root. (d): Additional thickening and cracking of reaction layer. (e): Unstable crack growth in the silicon film. [10]

The precise mechanism by which the surface oxide thickens under influence of cyclic stresses is as of yet unknown, but could be related to some form of stress-assisted diffusion or an increased oxidation reaction rate at the silicon/oxide interface. Compressive stresses occur in the silicon-oxide layer during oxidization because the molar volume of  $\text{SiO}_2$  ( $27 \text{ cm}^3/\text{mol}$ ) is larger than for Si ( $12 \text{ cm}^3/\text{mol}$ ). The corresponding reduction in oxidation rate as a silicon-oxide layer grows thicker has been partly attributed to the presence of these stresses because of a decrease in oxidant diffusion rate [42-44]. Additionally, tensile stresses in the silicon caused by the oxide can cause the oxidation reaction at the silicon/oxide interface to occur more quickly [45] (more details on oxidation of silicon can be found in Appendix B). When a cyclic load is applied, the compressive stresses in the oxide will be relieved during the tensile part of the loading cycle, which could result in less reduction in the oxidation reaction rate as the oxide grows thicker. Moreover, in combination with an applied compressive load in another part of the loading cycle, which increases the oxidation reaction, a rapid oxidation process could occur that results into the growth of thickened oxides in silicon at points of high cyclic stresses.

This reaction-layer model is consistent with the fact (i) that silicon fatigue is only seen in thin-film silicon, where a crack in the oxide layer can reach the critical size required to break the entire structure, and not in bulk silicon, where the critical crack size would be significantly larger than the oxide thickness, and (ii) that whereas silica is highly prone to moisture-induced fracture, silicon itself is not susceptible to either environmental cracking or fatigue.

The  $S/N$  results presented in Figure 3.3 for different devices and environments, together with the damage accumulation data (decay in resonance frequency with cycles) in Figures 3.4-3.5, and oxide layer thickness measurements in Figures 3.6-3.7, provide a considerable body of experimental evidence to support the reaction-layer mechanism. Specifically, the  $S/N$  data clearly show that the thin-film silicon fatigue effect occurs in ambient air in devices with both small initial oxide layers, i.e., the SUMMiT™ devices, as well as those with large oxide layers, i.e., from the MUMPs foundry, in this work from several fabrication runs. However, the SUMMiT™ devices appear to be stronger, a trend consistent with published tensile strength data for MUMPs and SUMMiT™ polysilicon [46,47]; this higher strength translates into higher overall fatigue resistance (at a given applied maximum stress, the lifetimes of SUMMiT™ devices were many orders of magnitude longer), presumably due to their thinner initial oxide films. Note that SUMMiT™ devices fabricated from a 2.50  $\mu\text{m}$  structural silicon layer (P21) have somewhat less fatigue resistance than those with a thinner (2.25  $\mu\text{m}$ , P3) layer. This is partly associated with the fact that devices fabricated from a thicker silicon film have more sidewall surface area and hence have a higher probability of containing micro-flaws; this statistical size effect means that samples consisting of thicker layers may display a lower strength even if the material is nominally similar [48]. More importantly, the sidewall surface roughness of the two devices is different: the root mean square (RMS) roughness of the P3 devices is ~90% of the RMS roughness of the P21 devices [47]. This difference in roughness allows for larger micro-flaws in the P21 devices than in the P3 devices.

Accompanying TEM characterization of the amorphous silica layer after fatigue clearly shows that regardless of the starting oxide thickness, the oxide layer in the vicinity of the notch thickens by a factor four to six times after  $\sim 10^{10}$  cycles in ambient or high humidity air (Figures 3.6-3.7). However, the maximum oxide thickness,  $h$ , varies substantially in devices with a different origin. Whereas notch-root oxides up to 100 nm thick were found in failed MUMPs devices, they were typically on the order of 20 nm thick in the SUMMiT<sup>TM</sup> devices. Recently, Pierron *et al.* [49] have proposed that reaction-layer fatigue can occur in two different scenarios: (i) the crack can stably grow inside the oxide until it reaches the critical crack size,  $a_c$ , i.e., the stress intensity for unstable crack propagation into the entire device is exceeded ( $a_c \leq h$ ), or (ii) where the crack can grow stably toward the silicon/oxide interface and change to instable growth as it reaches this interface ( $h = a_c$ ). In this second scenario the critical crack size is shorter than in the first scenario, because of an additional driving force for unstable crack advancement as it reaches the silicon/oxide interface [49]. For the MUMPs devices that have relatively thick initial (post-release) oxides ( $\sim 15$ -30 nm) which grow with cycling up to 100 nm, the first scenario applies because critical crack lengths of  $\sim 50$  nm will be reached within the oxide before the crack reaches the interface [46,49]. The SUMMiT<sup>TM</sup> devices, conversely, have thinner initial oxides (3-6 nm) which grow to a maximum of  $\sim 20$  nm thick; here instable cracking can only commence when the crack reaches the silicon/oxide interface, which allows for reaction-layer mechanism to occur in oxide layers down to  $\sim 15$  nm [49]. Note that in both these fatigue scenarios the only crack growth occurring in the silicon is of an unstable nature, which is consistent with the notion that bulk silicon does not fatigue, but micron-scale silicon does.

One critical experimental observation was that cycling MUMPs devices in higher humidity environments, specifically 95 %RH air, led to a definitive reduction in fatigue resistance in terms of shorter lifetimes (up to an order of magnitude) at a given applied stress, as compared to behavior in ambient 30-40 %RH air (Figure 3.3). This observation is again consistent with the reaction-layer mechanism as higher humidity would be expected to accelerate the stress-assisted oxidation and environmental cracking processes, leading to earlier failures. Indeed, a recent study on single crystal silicon has shown that fatigue damage accumulation occurs more rapidly in higher relative humidity conditions [50]. More importantly, no fatigue failures were observed *in vacuo*, even after cycling at stresses close to the fracture stress for more than  $10^{10}$  cycles (Figure 3.3). During these experiments, no change in resonant frequency could be detected, indicative of oxide growth or subcritical cracking. Furthermore, TEM layer thickness measurements of the oxides in both MUMPs and SUMMiT<sup>TM</sup> devices showed no local oxide thickening at points of high stress (Figures 3.6, 3.8). As minimizing the presence of oxygen and moisture in the test environment would act to suppress fatigue damage, i.e., oxidation and subcritical cracking in the oxide layer), these results are again fully consistent with the reaction-layer mechanism. It is also clear that models for thin-film silicon fatigue based on mechanical (non-environmental) fatigue mechanisms [14-16], are likely to be less relevant.

### 3.6 Summary and conclusions

Based on an experimental study of the very high-cycle fatigue ( $\sim 10^6$  to  $10^{12}$  cycles) of micron-scale polycrystalline silicon (free-standing) structural films (2-2.5  $\mu\text{m}$  thick) from

two different fabrication sources (MUMPs and SUMMiT<sup>TM</sup>), tested in ambient air (~25 °C, 30-40 %RH), high relative humidity air (>95 %RH), and high vacuum (<2 x 10<sup>-7</sup> mbar), the following conclusions can be made:

1. In contrast to bulk silicon which is not susceptible to fatigue, high-frequency (~36-40 kHz) cyclic loading of micron-scale polysilicon thin films in room air (at a stress ratio of -1) resulted in premature fatigue failure after ~10<sup>6</sup> to 10<sup>12</sup> cycles at applied maximum stresses less than the single-cycle fracture strength. Stress-life (*S/N*) curves were obtained, with lifetimes in excess of ~10<sup>11</sup> cycles being achieved when maximum stresses were typically ~70% of the fracture strength.
2. Such fatigue behavior in ambient air was observed in both MUMPs devices where the initial (post-release) oxide layers were large (~15-30 nm), and in SUMMiT<sup>TM</sup> devices where the post-release oxide thicknesses were much smaller (~3-6 nm). At a given applied (maximum) stress, lifetimes were many orders of magnitude longer in the higher-strength SUMMiT<sup>TM</sup> polysilicon films.
3. Fatigue behavior, and hence corresponding device lifetimes, were highly sensitive to the test environment. Lifetimes were observed to be up to an order of magnitude shorter in a high-humidity atmosphere (>95 %RH air), as compared to ambient air (30-40 %RH). No fatigue failures at all could be induced for tests run *in vacuo*, even after cycling at stresses close to the fracture stress for more than 10<sup>10</sup> cycles.
4. For both MUMPs and SUMMiT<sup>TM</sup> devices, cumulative fatigue damage, which has been related to local oxidation and subcritical cracking, could be detected throughout the fatigue life by a progressive decay in the resonant frequency of the device. Such



- behavior was always seen for tests in air, but never for tests *in vacuo* where no changes in resonance could be detected.
5. High-voltage and energy-filtered TEM imaging of the silicon oxide layers after cycling confirmed the occurrence of thickening of the oxide films, typically by 4 to 6 times, in the locally high stress region in the vicinity of the notch. The presence of nanoscale subcritical cracks were observed in these thickened oxide layers. Such behavior was not observed after cycling *in vacuo*.
  6. The presented fatigue results show conclusively that the reaction-layer fatigue mechanism for very high-cycle fatigue failure of micron-scale silicon films, where cyclic stress-induced delayed failures can occur at stresses less than the (single-cycle) fracture strength due to moisture-induced subcritical (stable) cracking within the oxide layer, is the governing mechanism for fatigue of micron-scale silicon. This mechanism is specific to thin-film silicon where cracks within the oxide can reach a large enough size to cause catastrophic failure of the entire device.

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## Chapter 4

# Wear in micron-scale polycrystalline silicon structural films

### 4.1 Introduction

The tribological properties (frictional, lubrication and wear properties), of materials used to fabricate microelectromechanical systems (MEMS) markedly affect their reliability (Chapter 1). Along with stiction [1,2] and fatigue (Chapter 2 and 3), wear is an important failure mechanism in these microsystems. Indeed, the system reliability of MEMS has received an increasing amount of attention [3,4] and there have been some attempts to propose micron-scale wear models for inherently brittle silicon, as will be shown in the following sections. However, the precise physical processes that cause wear in structural thin-film silicon in ambient air have yet to be conclusively determined and are therefore the focus of this study.

Early studies on the wear of single-crystal silicon wafers, using pin-on-disk testing, suggested wear mechanisms that have also been found in metals [5-8]: abrasion, chipping and flattening of protrusions, plasticity and delamination wear. One of the earliest *on-chip* MEMS micro-wear studies was performed by Mehregany *et al.* [9,10] where the change in the gear ratio of a n+-type polycrystalline silicon (polysilicon) MEMS wobble motor was used to indirectly determine wear. They observed a relatively

quick decreasing gear ratio after which it reached a more steady state, where the gear ratio remained constant or even increased slightly. Studying wear prevention by means of coatings, Ashurst *et al.* [2,11] have focused on adhesion, stiction, friction coefficients and surface contact angle of several molecular thin organic coatings on silicon MEMS and found that, because of low work of adhesion, the coefficient of friction could be lowered by more than one order of magnitude by applying these coatings on their polysilicon structures. Another test approach was chosen by Bhushan *et al.* [e.g. 12,13], who used atomic force microscope (AFM) scratch tests to determine tribological properties of different types of silicon films.

Several studies have investigated the friction coefficients<sup>3</sup> of silicon at different length scales. Table 4.1 shows the static and dynamic coefficients of friction of different types of silicon against several different materials at different length scales (macro-scale, micron-scale and nano-scale). Macro-scale dynamic friction coefficient values range from 0.1-0.69. Comparing those values to micron-scale dynamic measurements (0.1-0.5) reveals that these values are slightly higher at the high end of the range; however, for both size scales a large range of values is found. Nano-scale dynamic friction coefficient measurements range from 0.03-0.25 initially up to 0.6 after wear and are in a lower range than both macro and micron-scale measurements; specifically the lower bound is an order of magnitude smaller than the lower bound of the macro and micro-scale measurements. Comparing all these different studies of dynamic friction coefficients in silicon, there seems to be a general trend towards lower coefficients measured with decreasing length scale, although the significance of that trend is somewhat questionable because of the

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<sup>3</sup> The friction coefficient is the ratio of the frictional forces to the normal forces between two surfaces.

relatively small differences between the different length scales and the large range in data of the coefficients of dynamic friction for all length scales. This large spread is most likely caused by the fact that most tests are performed under different circumstances (e.g. testing methods, contact forces, environments) and also use a variety of different materials as the material against which the silicon slides.

Literature data available on macro-scale static coefficients of friction, also shown in Table 4.1, show values for silicon ranging from 0.18-0.6. Static friction coefficients collected at the micron-scale range from 0.25-1.1, whereas silicon coated with a FDTS monolayer (the initial situation in the case of the study presented in this chapter) gives a significantly lower value ( $\sim 0.1$ ). These static values are somewhat higher than the equivalent dynamic coefficients of friction, which is a well-known trend [14]. Despite this growing range of tribological studies of thin film silicon, the wear mechanisms are rarely the main focus, nor are these studies very conclusive on the active mechanisms. In the following sections three studies that do suggest more detailed wear mechanisms are discussed.



**Table 4.1:** Overview of silicon friction data from the literature, showing static and dynamic coefficients of friction at different length scales (SCS is single crystal silicon).

	Static Friction Coefficient	Dynamic Friction Coefficient	
<b>Macro-Scale</b>	<b>range: 0.18-0.6</b>	<b>Range: 0.1-0.69</b>	<b>Macro-Scale</b>
Si / SiO <sub>2</sub>	0.55(air)-0.39(vac) Pin on disc [15]	0.16-0.23 Ball on disc [20,13]	n-Poly / Al <sub>2</sub> O <sub>3</sub>
Si / SiN <sub>x</sub>	0.40(air)-0.35(vac) Pin on disc [15]	0.65-0.69 Ball on disc [13]	p-Poly / Al <sub>2</sub> O <sub>3</sub>
SCS / Al <sub>2</sub> O <sub>3</sub>	0.18(0.1N)-0.60(1N) Ball on disc [16]	0.3-0.46 Ball on disc [20,13]	Undoped Poly / Al <sub>2</sub> O <sub>3</sub>
SiO <sub>2</sub> / SiO <sub>2</sub>	0.43(air)-0.2(vac) Pin on disc [15]	0.33-0.37 Ball on disc [20,13]	Undoped SCS / Al <sub>2</sub> O <sub>3</sub>
		0.16-0.28 Pin on disc [17]	Si / Thin film rigid disk
		0.11-0.13 Flat on disc [18]	Flat glass / Si
		0.1-0.6 Pin on disc [19]	Si / Si
<b>Micro-Scale</b>	<b>range: 0.25-1.1</b>	<b>range: 0.1-0.5</b>	<b>Micro-Scale</b>
Poly / Poly	1.1(~11 uN) Sandia sidewall-device [21]	0.16(~1.6 uN) Sandia sidewall-device [30]	Poly / Poly
Poly / Poly	0.7 SCREAM sidewall friction [26]	0.2-0.4(15%RH) 0.1-0.3(90%RH) MUMPs motor [31]	Poly / Poly
Poly / Poly	0.5 Sidewall friction [27]	0.25-0.35 Wobble engine [28]	Poly / SCS
Poly / Poly	0.25 to ~1 Sandia nano-tractor [23]	~0.5 Ball-on-disc [29]	Poly / Steel
Poly / SCS	0.48-0.28(5.3-113 uN) Micro-features on disc [22]		
Poly / SiO <sub>2</sub>	0.85-0.70(5.3-113 uN) Micro-features on disc [22]		
SCS/SCS	0.6-1 Pin on disc [25]		
(L)FDTS	~ 0.1(~11 uN) Sandia sidewall-device [24]		
<b>Nano-Scale</b>		<b>range: 0.01-0.6</b>	<b>Nano-Scale</b>
		0.04-0.05 (10-150 uN) [17] AFM	Poly / Diamond
		0.04-0.05 [20] AFM	Poly/Si <sub>3</sub> N <sub>4</sub>
		0.04 to 0.42 [12] AFM (after scratching)	Poly / Diamond
		0.25 to 0.44-0.60 [12] AFM (after scratching)	p-Poly / Diamond
		0.03-0.04 (10-150 uN) [17] AFM	SCS / Diamond
		0.05 to 0.45 [12] AFM (after scratching)	undoped Si / Diamond
		0.04-0.07 [32] 0.03-0.04 [20] 0.03 (50-150 uN) [16] AFM	SCS / Si <sub>3</sub> N <sub>4</sub>
		0.05(1-15 uN)-0.20(20-50 uN) [16] AFM	SCS / Diamond
		0.01-0.04 [20] AFM	SiO <sub>2</sub> / Si <sub>3</sub> N <sub>4</sub>

#### 4.1.1 Specimen-on-disc testing

An extensive study of microfabricated surfaces in a macro-scale specimen-on-disc testing setup was performed by Beershwinger *et al.* [33,34]. Single crystal silicon, doped and undoped polysilicon and SiO<sub>2</sub> films were tested for wear. Surface roughness scans and wear rate as function of time were measured using a contact surface profiler. During testing single crystal silicon film surfaces became smoother. This behavior was explained by the brittleness of this material, which prevented plastic deformation from accommodating increased loads, but instead promoted asperity fracture, leaving a smoother surface with fewer large asperities. When the larger asperities were removed from the surface the wear rate dropped slightly, because increased real contact areas caused lower local stresses between the surfaces. This changed the regime from predominantly particle wear to atomistic wear. This behavior is consistent with conventional friction theory, in which the friction coefficient rises after a short wear-in period only to reach a maximum steady state value [14,35].

Wear tests on SiO<sub>2</sub> showed higher roughness, an increased wear rate and wear debris that was coarser than for single crystal silicon. It was suggested that the regime of particle wear was not yet over at the moment the tests were stopped. The authors suggested that the higher wear rate was consistent with the low modulus, hardness and toughness of SiO<sub>2</sub>, although they could not explain why the wear was so much higher than for single crystal silicon. However, although the toughness of silicon ( $K_{Ic} \sim 1 \text{ MPam}^{1/2}$ ) and silicon oxide ( $K_{Ic} \sim 0.8 \text{ MPam}^{1/2}$ ) are relatively similar, they do differ significantly in moist environments, where, due to stress corrosion cracking, the toughness for silicon oxide can drop to approximately  $0.25 \text{ MPam}^{1/2}$  [36]. This could

explain the difference in wear rate. For polysilicon the authors suggested that plastic asperity deformation was possible if the contact area was less than 40 nm, which would allow plasticity in this particular case, since scanning electron microscope (SEM) images showed that the asperity radii were between 50-100 nm, resulting in a contact area smaller than 40 nm. Furthermore the authors found that for polysilicon the initial wear rates were very high and eventually settling into a steady-state condition. Their data also showed that the wear rates for polysilicon are very dependent on contact pressure.

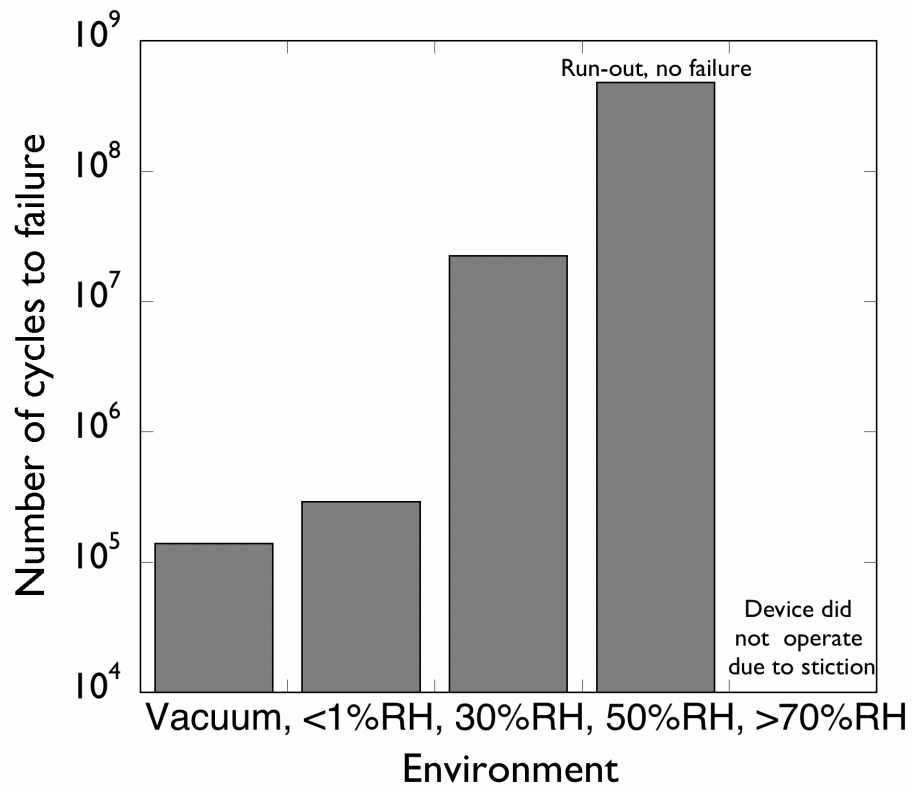
The effect of doping on the wear rate of silicon was also tested and showed that doped silicon wore less rapidly than undoped silicon. This was related to the higher bond strength in doped silicon in comparison with undoped silicon, but could also be related to different oxidation rates [33]. As with single crystal silicon and some of the polysilicon data, the wear rate was initially large and eventually reduced. This is consistent with the assumption of two wear regimes also seen in the study by Mehregany *et al.* [9,10] presented earlier and with macro-scale friction and wear theory [14,35]. Furthermore, it was suggested [34] that the mechanism for high contact pressure ( $F = 230 \mu\text{N}$ ,  $P = 9.6 \text{ kPa}$ ) in this case was different from the mechanism for lower contact pressure ( $F \approx 10\text{-}100 \mu\text{N}$ ,  $P \approx 0.4\text{-}5 \text{ kPa}$ ), because the wear rate at higher contact pressure was considerably higher than for lower contact pressures. Wear rates at these higher pressures were more consistent with wear rates found in macroscopic studies. The wear rate and surface roughness measurements as function of time gave useful additional information in the search for the mechanisms of wear. The possibility of different wear regimes explained most of the acquired data by means of existing friction and wear theory. However, all the tests were done with unidirectional sliding, which for some applications

might not be the most applicable situation. Finally, the counter surfaces consisted of different materials, which make comparison with most *on-chip* studies and applications more difficult.

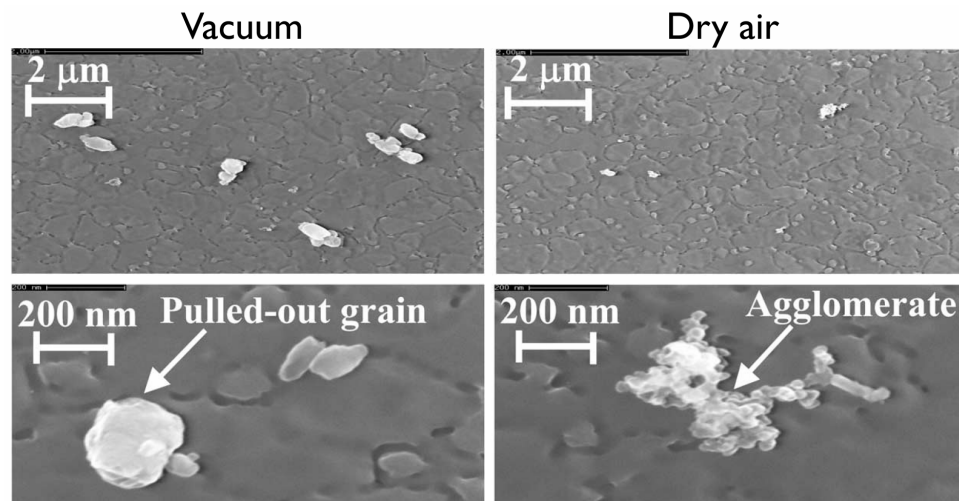
#### 4.1.2 Wear in a MEMS electrostatic output motor

Wear studies on a heavily doped n-type polysilicon electrostatic MEMS lateral output motor, fabricated at the MUMPs foundry [37,38], were performed by Patton *et al.* [39,40,41]. Sliding wear tests were performed in vacuum and compared with measurements in dry air, <1 % relative humidity (%RH), and moderately humid air, 30-50 %RH. The durability of the device increased with increasing humidity and the reliability in vacuum was slightly worse than in dry air (Figure 4.1). This trend was attributed to the absence of lubricating films in vacuum (either a native oxide or an adsorbed water layer), which resulted in a higher dynamic coefficient of friction [20]. The devices performed best at moderate humidity, because to the presence of a lubricating water film on the surface. At higher humidity, >70 %RH, excessive moisture prevented motion of the motor due to stiction.

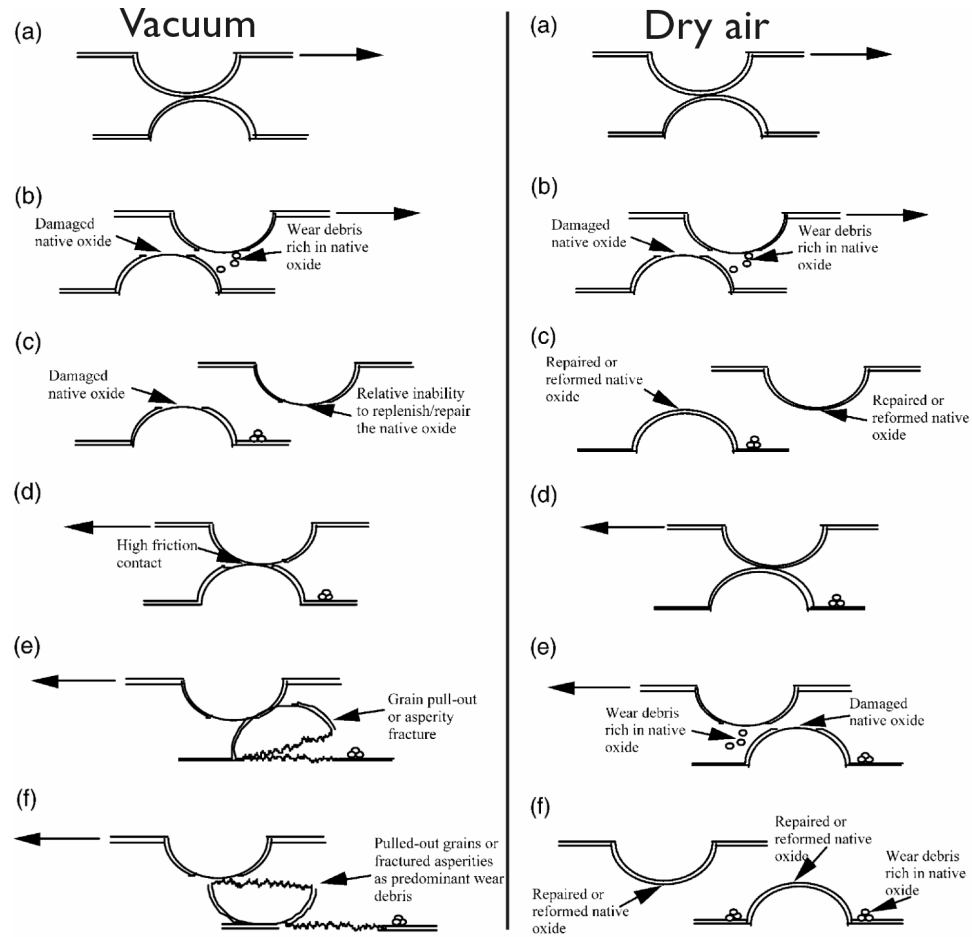
Observations of wear debris showed that more wear debris was generated in vacuum than in dry air. Furthermore, SEM images of wear debris in vacuum and dry air (Figure 4.2) revealed a distinct difference in wear debris morphology. Energy dispersive x-ray spectroscopy (EDS) measurements of wear debris showed the presence of oxygen in debris worn off in dry air, but not in debris created in vacuum. According to the authors this difference in morphology and composition suggested that different wear mechanisms were active in different environments.



**Figure 4.1:** Lifetime of a MEMS lateral output motor as function of the relative humidity. [41].



**Figure 4.2:** Morphology of wear debris created in vacuum and in dry air. [41]



**Figure 4.3:** Suggested wear models in vacuum (left) and in dry air (right). [41].

Two micron-scale wear mechanisms were proposed (Figure 4.3). Surface asperity interaction created adhesive wear of the native oxide layers, creating small wear particles. Since there was no regeneration of the oxide layer in vacuum, it exposed the underlying silicon. Lack of passivation of the surfaces led to bonding at asperity contact between the reactive silicon surfaces, resulting in higher friction. High local stress at asperities led to either asperity fracture or grain pull out. This mechanism predominantly yielded large silicon wear debris particles. In dry air, the process also started with wear of the native oxide layers. However, since the silicon surfaces were exposed to air, the native oxide

layer could regenerate, thus restarting the whole process. This mechanism would typically lead to small, oxidized silicon wear particles. A modified version of this mechanism could also be used for environments with higher %RH, with the additional lubricating effect of a thin water film on the surfaces that would lower the friction coefficient and increase the lifetime even more.

Although it is likely that in these different wear conditions different wear mechanisms are active, the evidence that is presented is not conclusive. For wear in dry air, the surface oxide layer has to regenerate fast enough to protect the silicon surface during the next cycle. Since the micromotors are operated at 1 kHz, this oxidation would have to happen very quickly. Even if the silicon surfaces are highly reactive and the temperature is locally raised due to friction, it is very unlikely that this is in fact the case. In addition, from the uncalibrated qualitative EDS and SEM data alone it cannot be determined if the wear debris in dry air is generated from SiO<sub>2</sub> or Si. At least part of the wear debris will be oxidized silicon particles. Asperity fracture by locally high stress concentrations seems like a valid wear mechanism in vacuum. However, there are no pits or wear tracks shown in the presented surface images to support the grain pull out mechanism. The grain size in these silicon films, fabricated in the MUMPs process, is of the order of several 100nm in diameter [36], similar in size as the debris particles, which would support the grain pull-out.

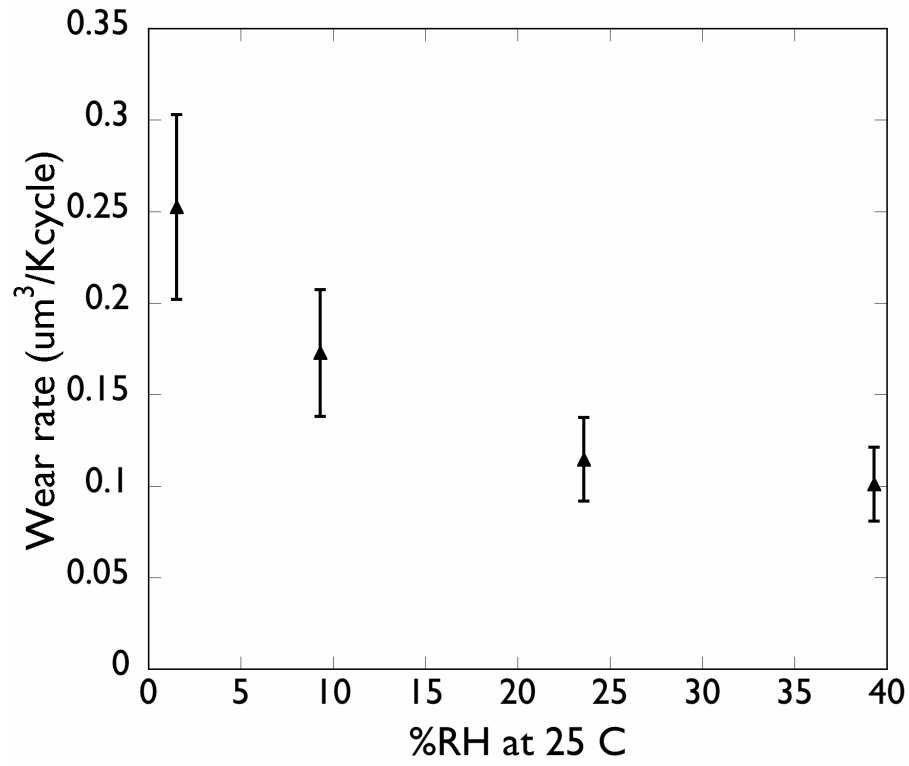
#### 4.1.3 Wear in a MEMS microengine

Tanner and coworkers studied rolling wear of a pin joint on a gear in an electrostatic MEMS microengine as function of driving frequency and humidity as well

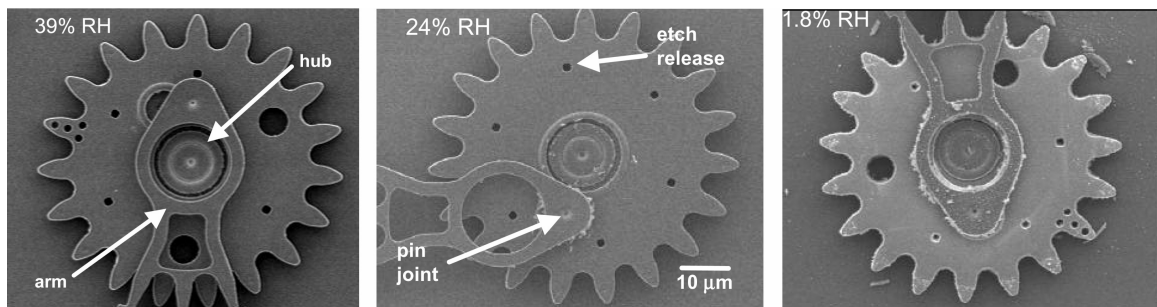
as sliding wear in a sidewall friction test device [28,30,42]. The polysilicon engines, fabricated in the Sandia SUMMiT<sup>TM</sup> process [43], were treated with different monolayer surface coatings to increase the lifetime. Among the author's findings were that after a large drop in lifetime when the environment was changed from 1.8 %RH to 10 %RH the engines had a slight increase in lifetime with increasing relative humidity. In contrast, the wear rate decreased monotonically when the relative humidity was raised (Figure 4.4). This data supports the theory that at higher relative humidity the system experiences less friction and wear, something that was also shown in the previous section and that can be explained by the formation of surface hydroxides that protect the surface from additional wear at higher %RH [28]. However, the initial drop in lifetime for specimens at 10 %RH in comparison with specimens run at 1.8 %RH cannot be explained by this theory.

SEM images of the engines after they had been cycled showed a large increase in the quantity of wear debris at low humidity (Figure 4.5). EDS analysis of the wear debris in a transmission electron microscope (TEM) showed that, next to silicon, oxygen was present in the debris particles. Since diffraction showed the particles were amorphous, the wear debris was suggested to be oxidized silicon. However, uncertainty about the initial size of the debris particles and the oxidation rate make this uncertain. The morphology of the wear debris was different with changing humidity. Higher humidity (39 %RH) gave 200-500nm agglomerates that strung together and formed longer chains. At lower humidity (1.8 %RH) debris consisting of small (~100nm) particles was found. These observations and the fact that at low humidity the device lifetime increased, although the amount of wear debris increased, suggested that different wear mechanisms were active at different relative humidities.





**Figure 4.4:** Influence of humidity on the wear rate; as determined from focus ion beam (FIB) cross sections of worn micro-engines observed by SEM. [28].



**Figure 4.5:** Visible wear debris on a gear and pin-joint at, from left to right, 39, 24 and 1.8 %RH. [28].

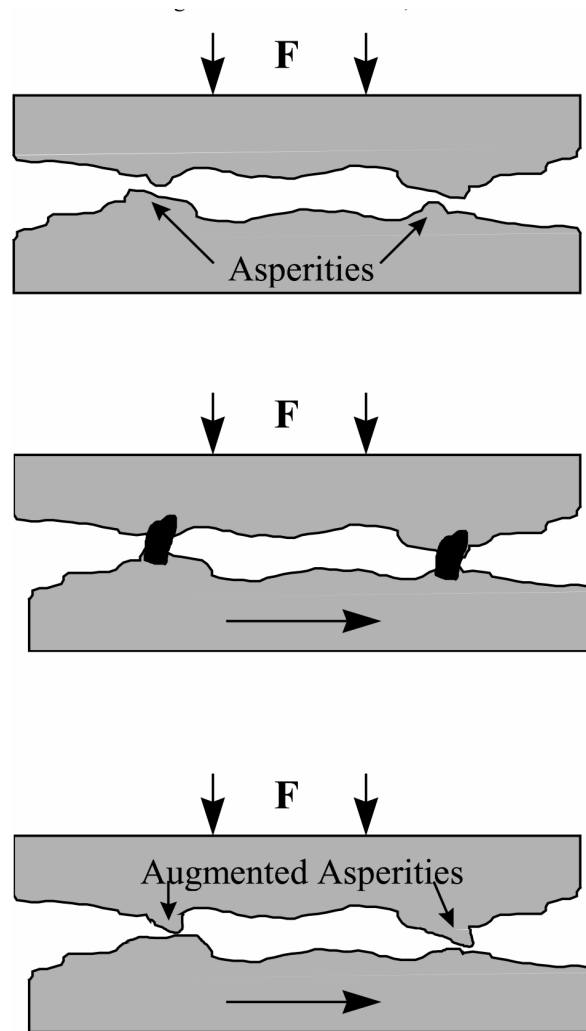
Tanner *et al.* assumed that micron-scale wear was caused by known mechanisms for macroscopic wear: adhesion, abrasion, corrosion, surface fatigue, deformation, impact

and fretting wear [42]. They ruled out several mechanisms, because the conditions were not favorable for these mechanisms to happen: for abrasive wear too little force was applied (in these devices wear tracks were known to form at driving forces around  $4\mu\text{N}$ , the presented test had forces  $\sim 3\mu\text{N}$ ); surface fatigue, deformation and impact wear also required larger forces; corrosion fatigue was ruled out since no corrosion by-products were observed and so was fretting wear<sup>4</sup>, because no micro-cracks had been observed. Ruling out all other mechanisms, an adhesive wear model was suggested to be responsible for failure of the microengines (Figure 4.6). Asperities on two wearing surfaces touched and after plastic flow were cold-welded together. Because of the continuing movement of the surfaces, the welded asperities broke, leading to augmented asperities and wear debris. Adhesive wear models were quantitatively compared with the data from a driving frequency dependent lifetime test and showed a good fit [42].

Although by ruling out other mechanisms adhesive wear seems an obvious choice, there are certainly some questions that arise. The role of plastic flow for example, which in silicon generally only occurs at very high pressures ( $> 10\text{ GPa}$  in compressive indentation tests) [44]. In addition, this model would not explain why the engines which show the most wear debris in dry air would have the longest lifetime. Also, it is unclear if the surface roughness of these polysilicon devices coincides with the wear debris particle size, which would be expected in the case of asperity fracture.

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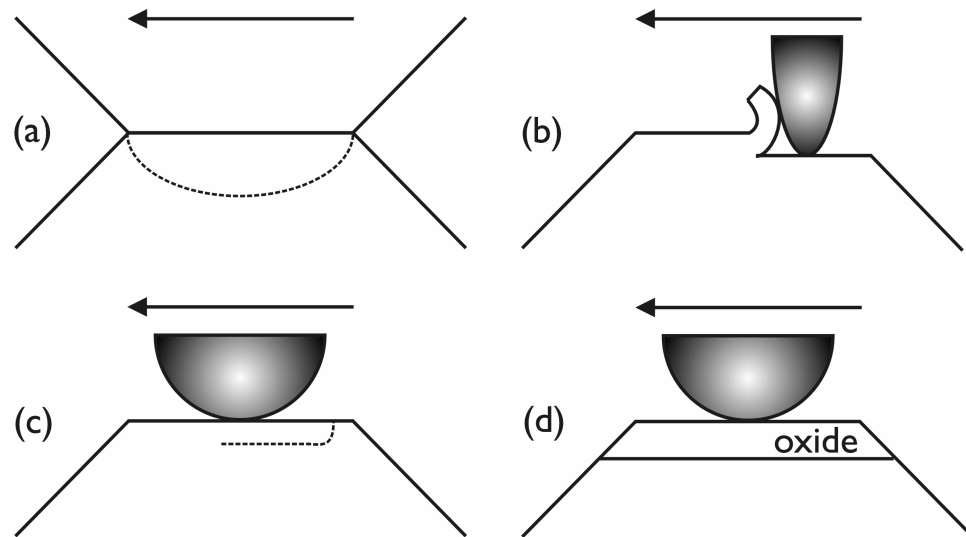
<sup>4</sup> Fretting wear occurs when parts experiencing fluctuating loads that lead to microcracks and fatigue failure



**Figure 4.6:** Suggested adhesive wear model by Tanner *et al.* [42].

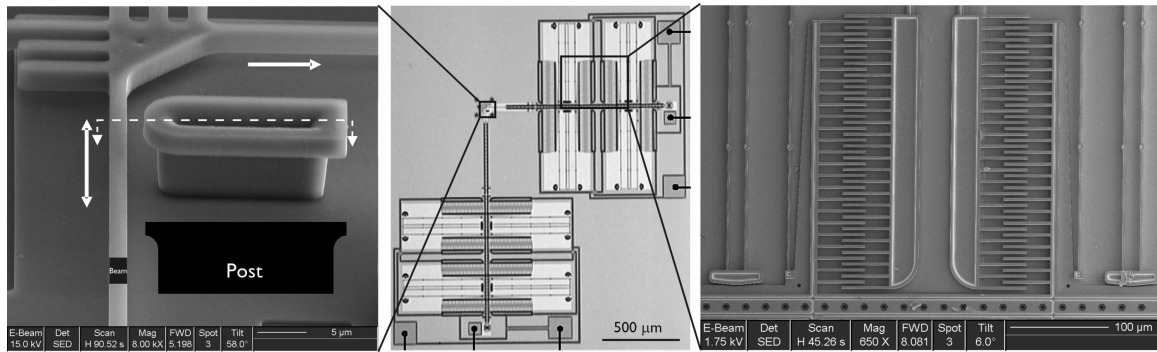
In the present study, presented in the remainder of this chapter, *on-chip* MEMS testing and a suite of electron and infrared microscopy techniques were used to investigate micron-scale wear in polycrystalline silicon structural films in ambient air. Examination of wear debris and worn surface regions as well as static friction coefficient measurements leads to a proposed mechanism describing wear at the micron-scale. When looking for active wear mechanisms in these silicon structural films, the focus will specifically be on the four distinct mechanisms known from tribology theory: adhesive

wear, abrasive wear, delamination wear (a.k.a. surface fatigue) and corrosive wear (Figure 4.7). Adhesive wear (Figure 4.7(a)) occurs when two surfaces adhere because they come into intimate contact, but because of continuing motion separate again, transferring material from one surface to another and creating wear debris in the process by fracture of particles originating from one of the surfaces. Abrasive (Figure 4.7(b)) wear occurs when surface asperities, or wear particles, plow into the surface and create wear tracks and further debris. A more complex mechanism is delamination wear, or surface fatigue (Figure 4.7(c)), which occurs by the initiation and propagation of sub-surface cracks ultimately leading to flake-like debris particle formation. Finally, wear aided by chemical reactions is called chemical wear, in its most common form this would be corrosive wear (Figure 4.7(d)).



**Figure 4.7:** Wear mechanisms: (a) adhesive wear, (b) abrasive wear, (c) delamination wear/surface fatigue and (d) corrosive wear. The arrows indicate the sliding directions.

## 4.2 Experimental procedures



**Figure 4.8:** Polysilicon side-wall friction test device fabricated at the Sandia SUMMiT™ process. The device produces two-axis motion provided by electrostatic actuation of interdigitated comb drives used to pull a beam against a post and rub the two surfaces.

To study active mechanisms in sliding wear, n-type polysilicon MEMS side-wall friction test specimens are used with a perfluorodecyltrichlorosilane,  $\text{CF}_3(\text{CF}_2)_7(\text{CH}_2)_2\text{SiCl}_3$ , mono-layer coating<sup>5</sup> fabricated using the Sandia National Laboratories SUMMiT™ process (Figure 4.8) [30,43]. Specifically, two electrostatic comb-drive actuators create motion in two orthogonal directions. Applying a DC voltage to one of the actuators pulls the beam against a post, with a force that can be calculated using Equation 3.1; sinusoidal AC signals leading to the other, perpendicular, comb drive then cause the beam to rub back and forth against the post (Figure 4.8). To determine the normal forces between the beam and the post during the wearing process, the devices were calibrated first. By noting the applied DC voltage in the normal comb drive until it touches the post and using elastic beam bending theory, the normal force can be

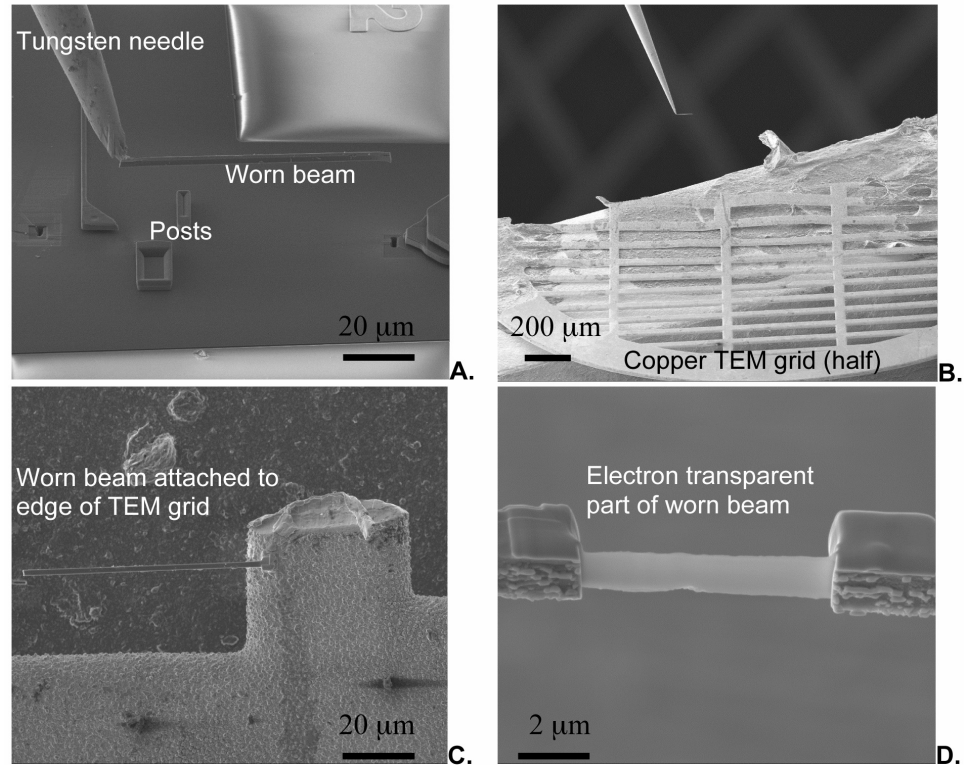
<sup>5</sup> Released via the following steps in solution at room temperature: release etch (buffered HF); rinse with DI water; oxidize with  $\text{H}_2\text{O}_2$ ; rinse with DI water; transfer to isopropyl alcohol, then iso-octane; transfer to 1 mM solution of the monolayer in iso-octane; hold in solution for 2 hours; transfer to neat iso-octane; to isopropyl alcohol; to DI water; remove from DI water and air dry on class 10 clean bench

determined as function of the applied voltage to the normal comb drive. The same devices can also be used to determine the static coefficients of friction by applying a normal force by means of a normal DC voltage and increasing the tangential force by ramping a second DC voltage signal ( $\sim 1$  V/s) and noting the point where the beam slips along the post. More details on the calibration procedure and the calculations of the static coefficient of friction can be found in Ashurst *et al.* [21].

After wearing the devices in ambient air (30-50% relative humidity, 22-25 °C) under a normal surface force of  $\sim 1$ -3  $\mu\text{N}$  at frequencies of 100 to 400 Hz with a sliding amplitude of  $\sim 5$ -15  $\mu\text{m}$ , SEM images of worn surfaces and the associated wear debris were used to determine the morphology of the worn areas. The SEM imaging was performed using both a JEOL 6340F Field Emission SEM (FESEM) and a FEI Strata DB235 Dual Beam Focused Ion Beam (DBFIB). EDS was further utilized to provide qualitative information on the chemical composition of the debris particles and beam surface.

FIB sample preparation techniques [45] followed by TEM observations, utilizing both a 300 kV JEOL 3010 (LaB<sub>6</sub> filament) and a 200 kV Philips CM200FEG (field emission gun), were used to acquire more detailed information on the wear debris and worn surfaces. After removing worn beams from the devices and thinning them to electron transparency, worn areas of the beam were observed by TEM and the debris analyzed using both imaging and diffraction modes, the latter giving information regarding the crystal structure. Additionally, analytical TEM, which combines quantitative chemical analysis with high spatial resolution, was used to analyze the chemical composition of the wear debris and worn areas in the beam. In this case, EDS in

combination with a reference sample of known composition was used to acquire quantitative information. The reference  $\text{SiO}_2$  TEM sample was prepared from a silicon-on-insulator (SOI) wafer by chemically etching the silicon handle wafer from the back and the silicon device layer from the front, using standard planar-view silicon TEM sample preparation techniques [46].



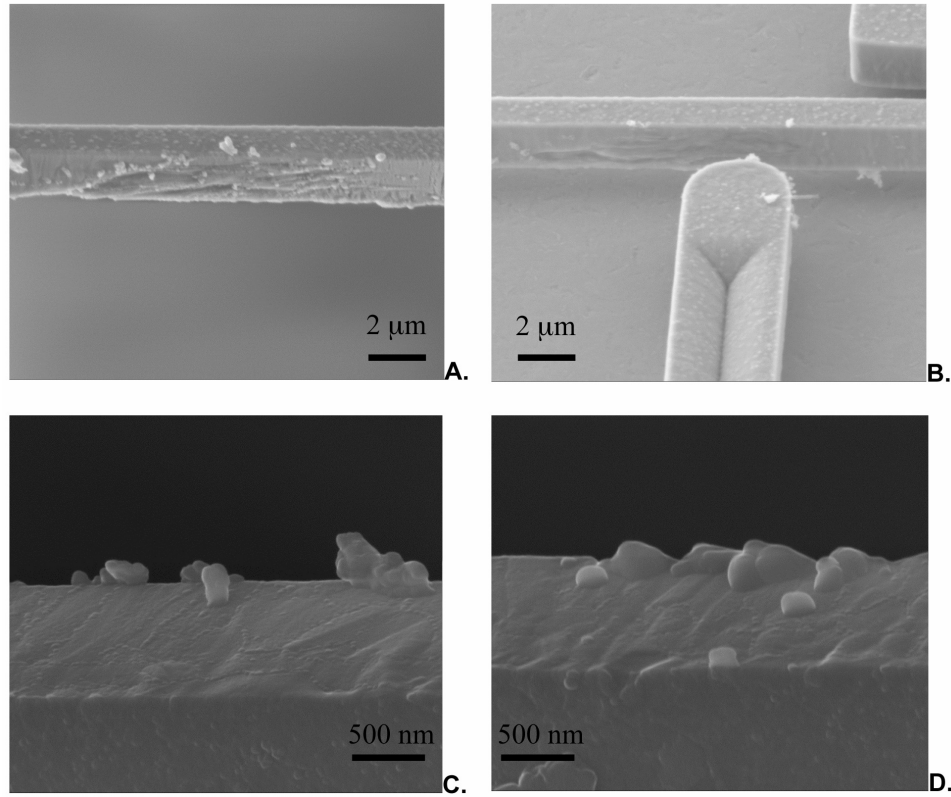
**Figure 4.9:** FIB lift-off TEM sample preparation, using Dual Beam FIB mounted with an Omniprobe (tungsten needle in the two top images). (a): Worn beam is cut from device and platinum-welded to the Omniprobe. (b): Sample is moved to half TEM grid (3 mm diameter circular copper grid). (c): Sample attached to TEM grid, (d): Beam thinned to ~100 nm thickness by ion beam in worn region (bottom of sample; edge of thin part); note the protective platinum coating on the facing side that was deposited on the surface before the beam was thinned to protect the sample during thinning. All images are taken using electron imaging at 5 kV.

Worn beams of the sidewall devices were cut out of the device using the FIB and moved to (half a) copper TEM sample grid (Figure 4.9) by means of a sharp tungsten micromanipulation needle (OmniProbe), to which the beams were (temporarily) welded using platinum. FIB thinning of these beams was performed after depositing protective layers of platinum on the surface exposed to the ion beam during thinning to electron transparency. First a platinum layer was put down using the electron beam (with minimal surface damage) to protect the sample from damage during deposition of the second, thicker, layer with the ion beam. To thin the beam, slices perpendicular to the worn surface were milled off, starting from the side of the beam that was protected with platinum, i.e., opposite to the side that had been worn. This was necessary to prevent ion implantation during thinning and subsequent damage of the worn surface.

Finally, the devices were run while imaged in an infrared (IR) microscope-type system (courtesy of Manera Systems Corporation, Fremont) to determine the magnitude of any temperature increases caused by friction in the structures during actuation. The IR system employed liquid nitrogen cooled detectors (InSb based), implemented on a proprietary inspection platform. This system has a spatial resolution of 5  $\mu\text{m}$  and a temperature resolution of 10 mK. Using a semi-quantitative temperature model, an estimate of the local temperature increase was determined.



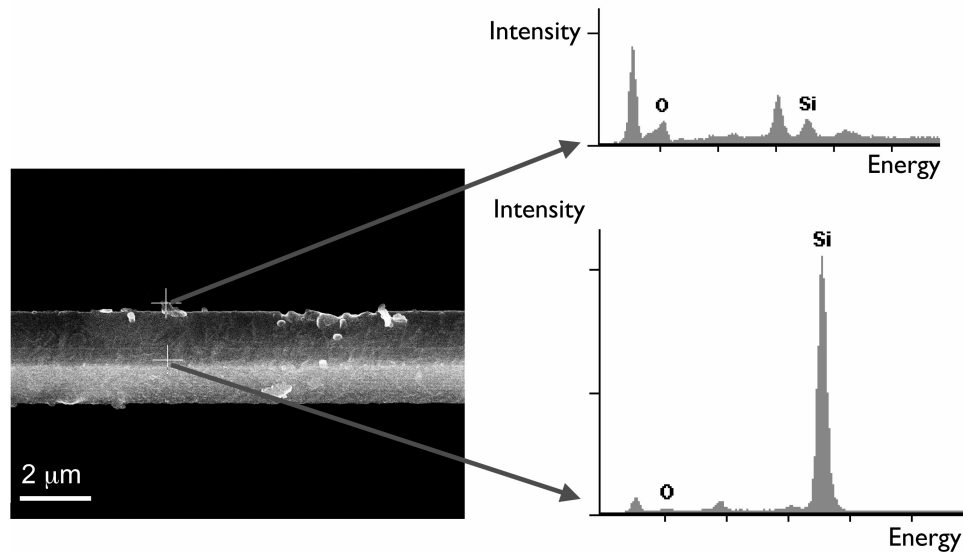
### 4.3. Electron microscopy debris and surface characterization



**Figure 4.10:** Typical SEM images of different worn devices after wearing, (a)  $\sim 3 \times 10^6$  cycles, (b)  $\sim 5 \times 10^5$  cycles; (c), (d) wear debris ( $\sim 100$ - $500$  nm in size) on the surface of a worn beam after lift-off from the chip. In (c) and (d) the worn surface is on a face of the beam that is not directly visible; debris particles however are clearly visible. (a), (b) are taken at 5 kV and (c), (d) at 18 kV.

SEM images of worn silicon beam surfaces and wear debris, shown in Figure 4.10, were used to deduce the morphology of the wear particles and worn surfaces. The debris and worn surface morphology appeared similar for devices that were run from hundreds of thousands to several millions of cycles under similar conditions; only the total visible surface wear damage increased as the number of cycles increased. The debris particles, which varied in diameter from a minimum of  $\sim 50$ - $100$  nm to a maximum of  $\sim 500$  nm (Figure 4.10(c),(d)), exhibited a relatively spherical morphology, unlike the

more flake-like debris that is often encountered with delamination wear (surface fatigue) [47]. Delamination wear is also unlikely because subcritical cracking in silicon does not occur and fatigue effects are associated with cracking in silicon oxides (Chapter 3). A reaction-layer delamination wear mechanism for subcritical cracking would require sub-surface oxidation, which seems highly unlikely. The worn surface of the beam did show evidence of long plow tracks (several  $\mu\text{m}$  in length), with a width of  $\sim 100\text{-}400\text{ nm}$  (Figure 4.10(a),(b)). This is an order of magnitude larger than the inherent root mean square roughness of the sidewalls ( $\sim 10\text{-}15\text{ nm}$ ) [48,49], but is of the same order of magnitude as the wear debris, suggesting that their formation is associated with abrasive wear, caused by the debris particles.

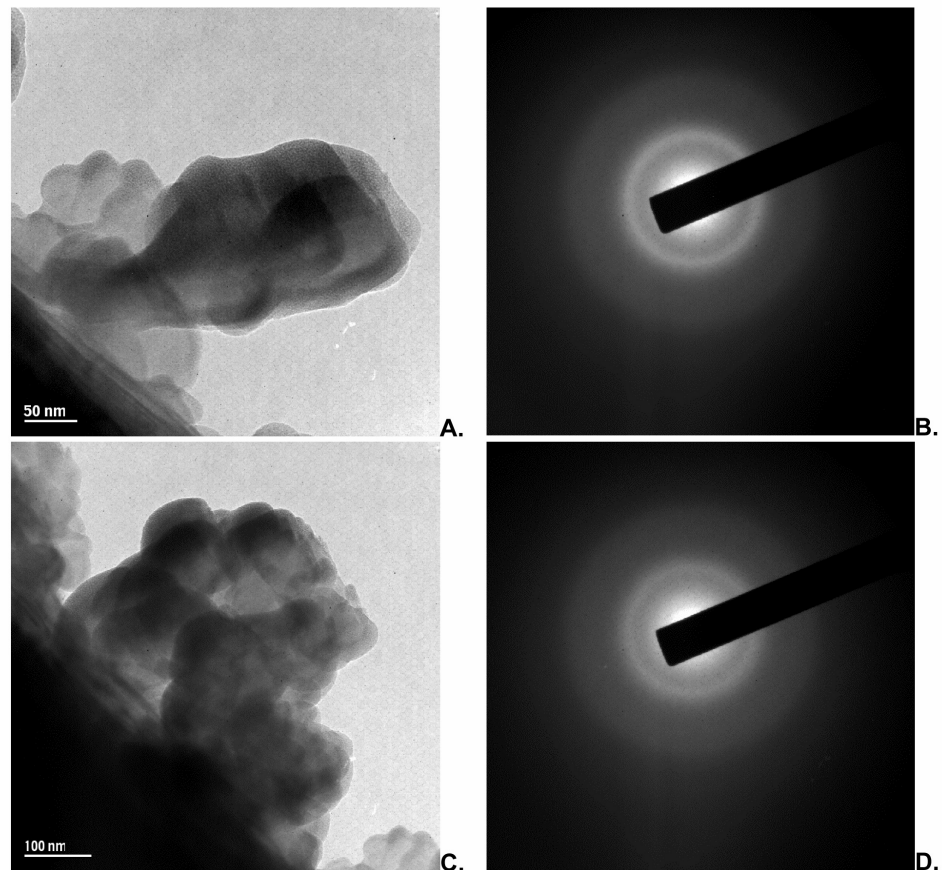


**Figure 4.11:** SEM EDS of the worn surface of the silicon beam at  $\sim 30$  degree tilt, (bottom right) and of wear debris (top left). The debris particles appear to be  $\text{SiO}_2$ , although no reference sample was used; thus it is not possible to quantitatively calibrate these values. Substantial C and Al peaks are visible in the spectrum of the debris; however, the Al is from the sample holder and the C is a typical artifact caused by beam-induced contamination.

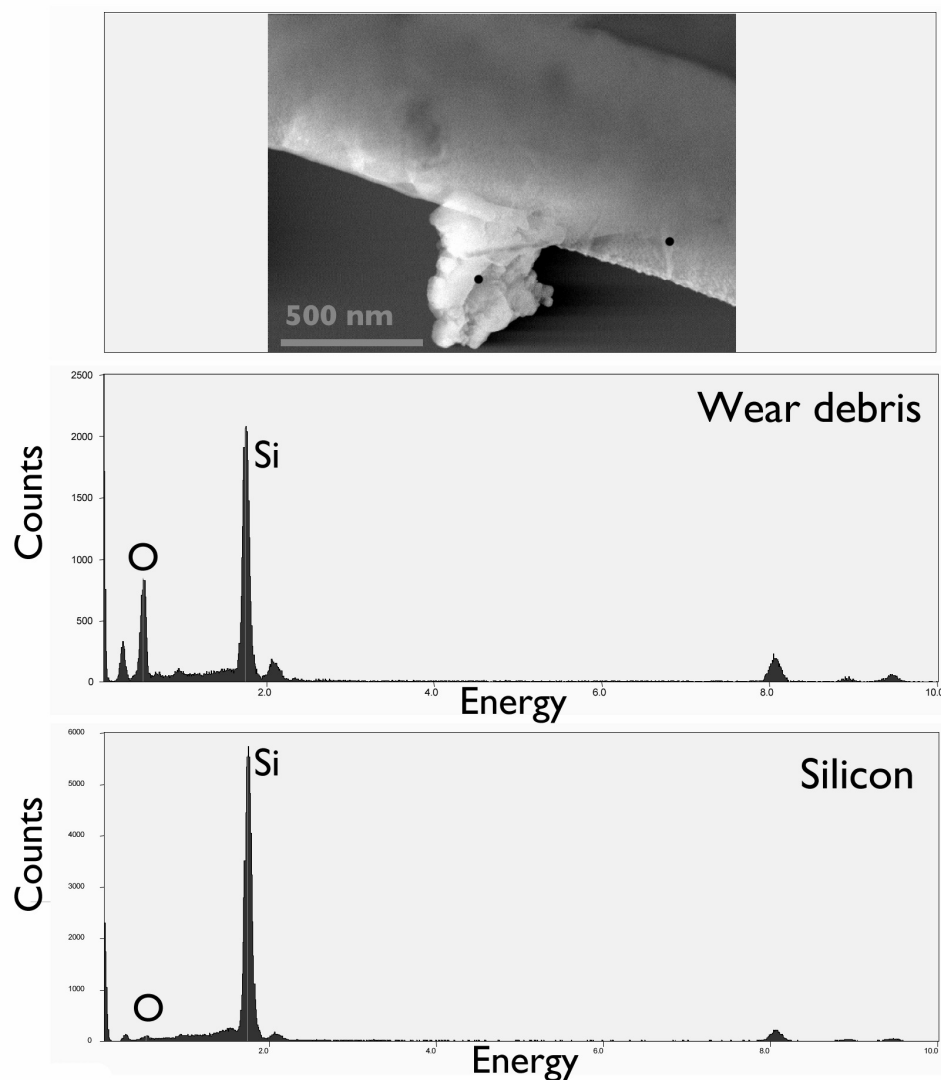
An approximate chemical composition of the wear debris and the worn surface was determined by EDS in the SEM. As expected, the central region of the beam was found to be pure silicon; however, a higher oxygen content was found in the wear debris, which suggests that the debris is at least partially oxidized silicon (Figure 4.11). Indeed, semi-quantitative analysis (based on simulated spectra embedded in the software program used) of these spectra revealed atomic fractions consistent with the debris being  $\text{SiO}_2$ ; however, because of the lack of an appropriate standard, the precise chemical composition could not be conclusively determined. The EDS spectra also show a clear carbon peak to the left of the oxygen peak, for both the worn surface and wear debris; additionally, an aluminum peak is visible in the spectrum for the debris particle. The former is an inherent effect of electron microscopy, where carbon is deposited on the sample surface during imaging [50]; the latter is caused by the aluminum sample holder. No traces of other elements from the coating were found, suggesting that the mono-layer surface coating only delays wear. This is consistent with the fact that for bare silicon devices the debris morphology looks similar, but takes longer to form in large quantities.

Bright-field TEM images and selected-area diffraction (SAD) patterns, shown in Figure 4.12, indicate that the debris particles are amorphous. Diffuse rings were found around the forward scattered beam in the diffraction patterns across the particle (Figure 4.12(b),(d)). It also appears that all the larger debris particles (up to ~500 nm in size) consist of an agglomeration of smaller particles (~50-100 nm). Figure 4.12(a),(c) show different contrast inside the agglomerates, which are bounded by shapes similar to the smaller debris particles. These smaller particles are ~50-100 nm in diameter and do not appear to be made up of even smaller particles, as one might expect from atomic-scale

wear of the top silicon dioxide layer and eventually the silicon itself. These observations lead to two conclusions: (i) wear occurs by removal of 50-100 nm particles and does not occur by atomic-scale grinding, and (ii) because the inherent grain size of the polysilicon in the beam is ~500 nm (this can be deduced from Figure 4.14), this wear debris must be generated by fracture through the grain.



**Figure 4.12:** Typical TEM bright-field images (a), (c) and accompanying diffraction patterns (b), (d) of debris particle agglomerates, show the particles to be amorphous. The dark areas in the bottom left of both images are the surface of the worn beam.



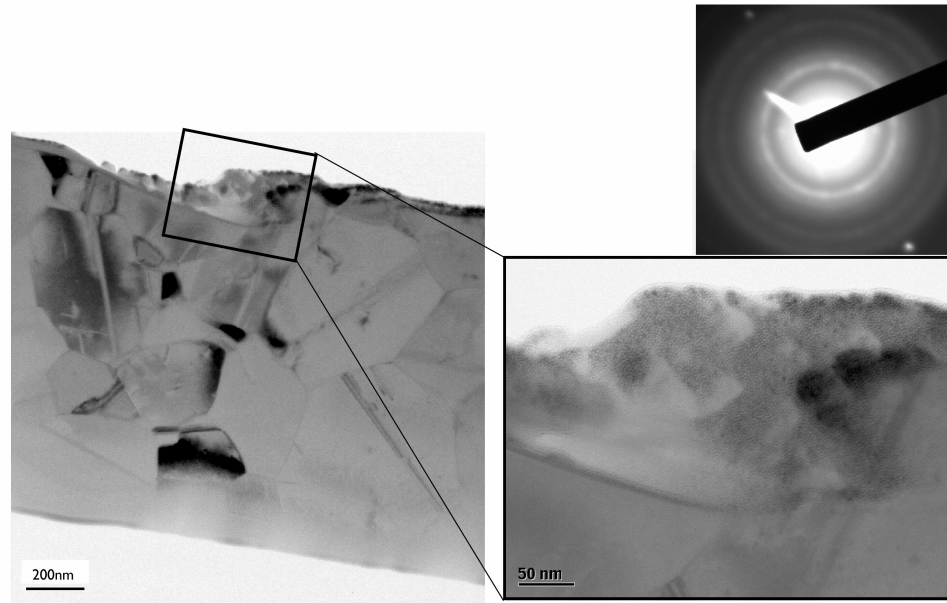
**Figure 4.13:** TEM EDS of wear debris and beam. The dots in the image, which show the beam and a large debris agglomerate on the surface, indicate where the two X-ray spectra were acquired. The beam consists of silicon, whereas the debris particle has a much higher oxygen concentration.

TEM EDS analysis confirmed that the oxygen content of the debris particles was higher than inside the beam (Figure 4.13). Quantification of these EDS results using a reference  $\text{SiO}_2$  sample revealed a silicon-oxygen atomic ratio of ~50:50 in the middle of the particles but ~34:66 at the edges. Because the outer edge of the particle does have the

1:2 silicon to oxide ratio and because these oxides are likely formed at temperature not much higher than room temperatures, which will be shown in the next section, this suggests that although the debris particles are fully amorphous, they do not entirely consist of  $\text{SiO}_2$  (for which a 33:66 ratio would be expected for the entire particle). Accordingly, it can be concluded that the particles oxidize heavily when they are worn off, which is consistent with situations that can promote additional oxide growth (Appendix B), and are comprised of an amorphous  $\text{SiO}_2$  shell and an amorphous Si or  $\text{SiO}_x$  core. It is not possible at this stage to define with complete certainty if the core is Si or  $\text{SiO}_x$ , when the particles become amorphous or what causes this to happen, although it most likely occurs after they are removed from the grain and could be aided by high local contact stresses (which can be expected to be as large as several GPa [51]).

It was also apparent that sections of the worn beam exhibited a surface layer with a microstructure that was quite distinct from the rest of the beam, as shown in the TEM bright-field image in Figure 4.14. (Here the top edge is the surface where the beam has been worn and where a section of this surface layer is shown; at the bottom edge, the remainder of the protective Pt layer can be seen). These surface layers varied in their in-plane thickness from ~20 nm to almost 200 nm, and appeared to be amorphous, whereas the beam itself is populated with ~500 nm sized polycrystalline silicon grains. Closer investigation revealed that this surface layer is actually nano-crystalline, as typified by the region in Figure 14 where the layer is thicker (~200 nm). Because of the sharp rings visible in the diffraction pattern, it can be concluded that there are numerous small crystals present in this relatively small volume. These nano-crystals are much smaller than the overall grain size and are even smaller than the debris particles. Control samples

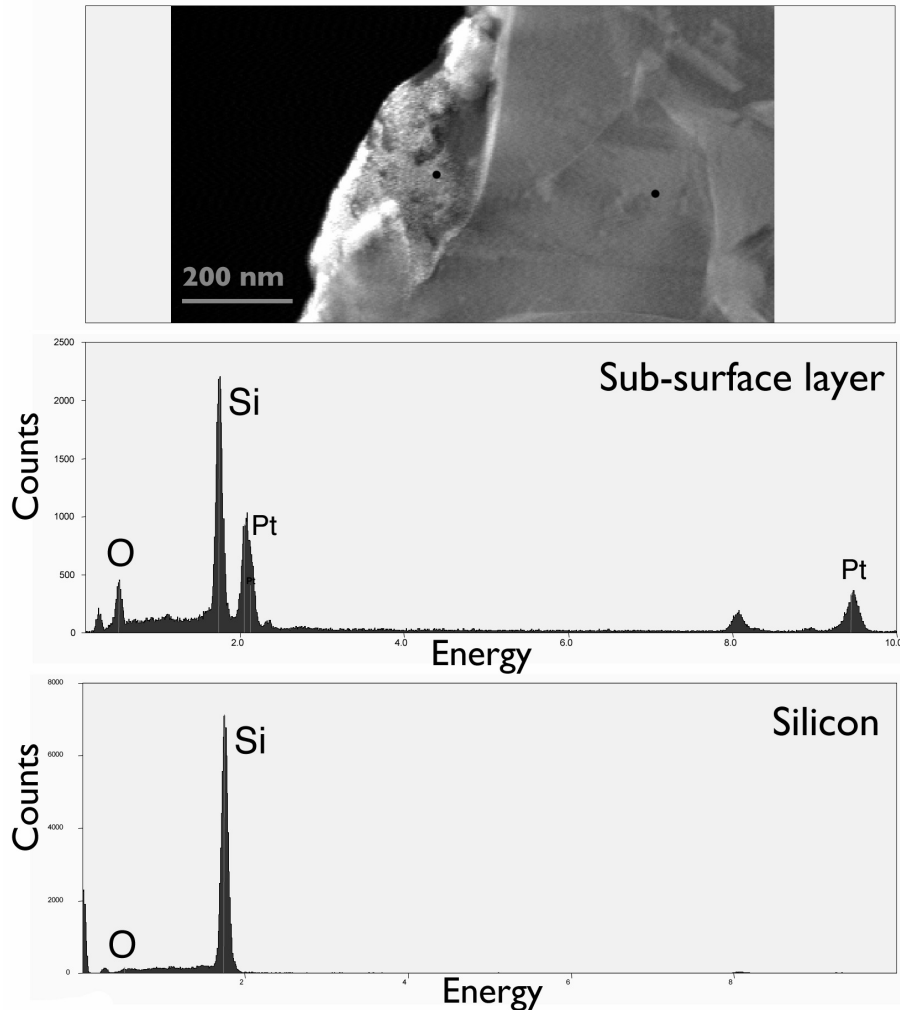
of areas that were not subject to wear confirmed that the microstructure inside the beam looked similar in both cases. However, these control samples showed no evidence of a surface layer with a different microstructure, as was observed in worn areas.



**Figure 4.14:** TEM bright-field image and selected area diffraction (SAD - upper right) of surface layer in worn area of beam. The image shows that the top surface layer, which has been worn, has a different microstructure than the beam. The rings in the SAD pattern show that this thin surface layer is nano-crystalline.

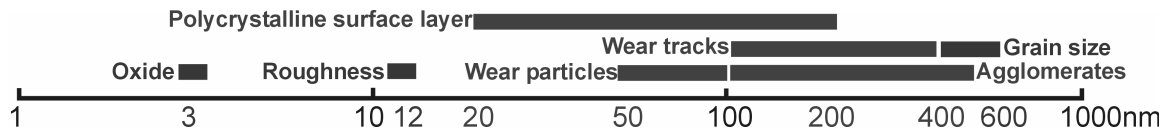
EDS measurements revealed that the oxygen content was higher inside this surface layer than in the rest of the beam (Figure 4.15). Quantitative analysis of the EDS results with respect to a  $\text{SiO}_2$  reference sample shows that the layer is not fully  $\text{SiO}_2$  ( $\text{Si}:\text{O} = 65:35$  atomic percent in the marked area; in other areas of the layer  $\text{Si}:\text{O}$  atomic percent ratios of 80:20 have been recorded). This is consistent with the fact that the layer is actually nanocrystalline, with Si as the dominant species, although with a significant degree of oxidation. These results suggest that smaller ( $\ll 100$  nm) partly-oxidized debris particles, created during actuation, become attached to the beam and lead to the formation

of this surface layer. These particles could be originating from the initial surface asperities, which were ~10-15 nm in size, or could be smaller debris particles that fractured at the same time that larger wear particles were created. Finally, all the listed length scales of features measured during the electron microscopy investigation presented above have been recapitulated in Figure 4.16.



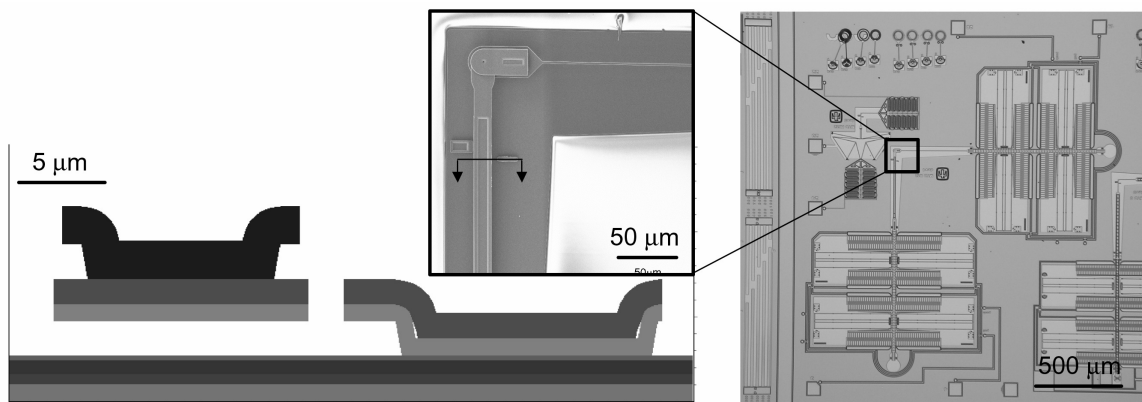
**Figure 4.15:** TEM EDS of surface layer. The dots in the image, which show part of the worn surface layer and the microstructure of the silicon beam, indicate where the X-ray spectra were acquired. The beam consists of silicon, whereas the surface layer has a higher oxygen concentration. Note: the platinum peak is an artifact of the FIB sample preparation method, and represents ~5 atomic percent of the surface composition.





**Figure 4.16:** Logarithmic overview of the length scales of the different features found in worn polysilicon side-wall friction devices, as they were presented in the previous sections.

#### 4.4 Infrared microscopy temperature measurements



**Figure 4.17:** Overview of alternative friction devices design used for the infrared experiments. The beam that wears against the post is wider to facilitate easier observation.

IR microscopy images were obtained during device operation to gather information on the possible local temperature increases at wearing surface and with that temperature increase the likelihood of the occurrence of plastic deformation. To accommodate for the 5  $\mu\text{m}$  spatial resolution of the IR system a wear device with a wider wearing beam width was used for these experiments (see Figure 4.17 for device layout, post/beam area and device cross-section). Figure 4.18 shows an increase in contrast, representing temperature changes in the beam that is being worn, as well as in the comb

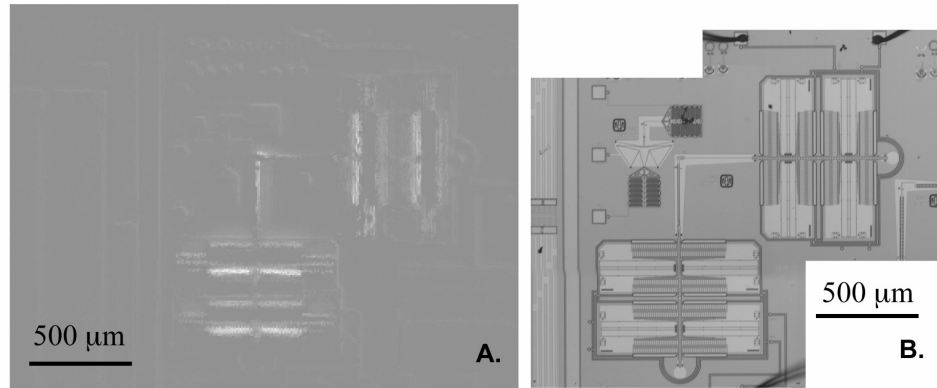
drives. Based on temperature models used with similar experiments with this IR microscope system [36], the increase in the temperature experienced by the MEMS parts at the point of contact is estimated to be  $\sim 9$  K, the order of magnitude of which is consistent with rough estimates calculated using simple flash temperature models [52].

$$\Delta T = N \frac{\mu F v}{4 r K} = 3472 \frac{0.3 \cdot 3 \mu N \cdot 4 \text{ mm} / \text{s}}{4 \cdot 6 \text{ nm} \cdot 124 \text{ W} / \text{mK}} = 4.2 \text{ K} \quad (4.1)$$

Where  $\mu$  is the friction coefficient,  $F$  the load between the two surfaces,  $v$  velocity of beam with respect to the post (calculated from the operating frequency and the wear track length),  $r$  equivalent contact radius,  $K$  thermal conductivity of silicon [37] and  $N$  the estimated number of contacts (calculated using an assumed apparent contact area,  $\sim 2 \mu\text{m}^2$ , containing asperities of  $\sim 24 \text{ nm}$  diameter).

Interestingly enough similar temperature rises are also seen at the comb drive, presumably because of frictional energy caused by viscous damping in the narrow gaps of the quickly moving comb drive. Such variations in temperature are unlikely to promote extensive dislocation plasticity, which is generally observed above  $\sim 500$  °C [53]. It is feasible that more significant temperature increases are generated at very localized regions, e.g., at sub-micrometer levels, such as the frictional contact area and asperity/asperity or debris particle/surface interaction areas; however, such localized regions are beyond the spatial resolution limit ( $\sim 5 \mu\text{m}$ ) of most, if not all, IR microscope systems. Additionally, the TEM images of FIB cross-sectioned samples did not reveal any evidence of additional dislocation pile-ups below or in the surface layer after wearing

(Figure 4.14). This strongly suggests that dislocation plasticity is indeed not an active component in the mechanism for wear of silicon at these length-scales.



**Figure 4.18:** IR microscopy image of operating wear device (a): ambient air, 3 min at 200Hz. The image shows a small temperature increase in the silicon beam and comb drive. For comparison, an optical micrograph of the same device is given (b).

## 4.5 Coefficients of static friction

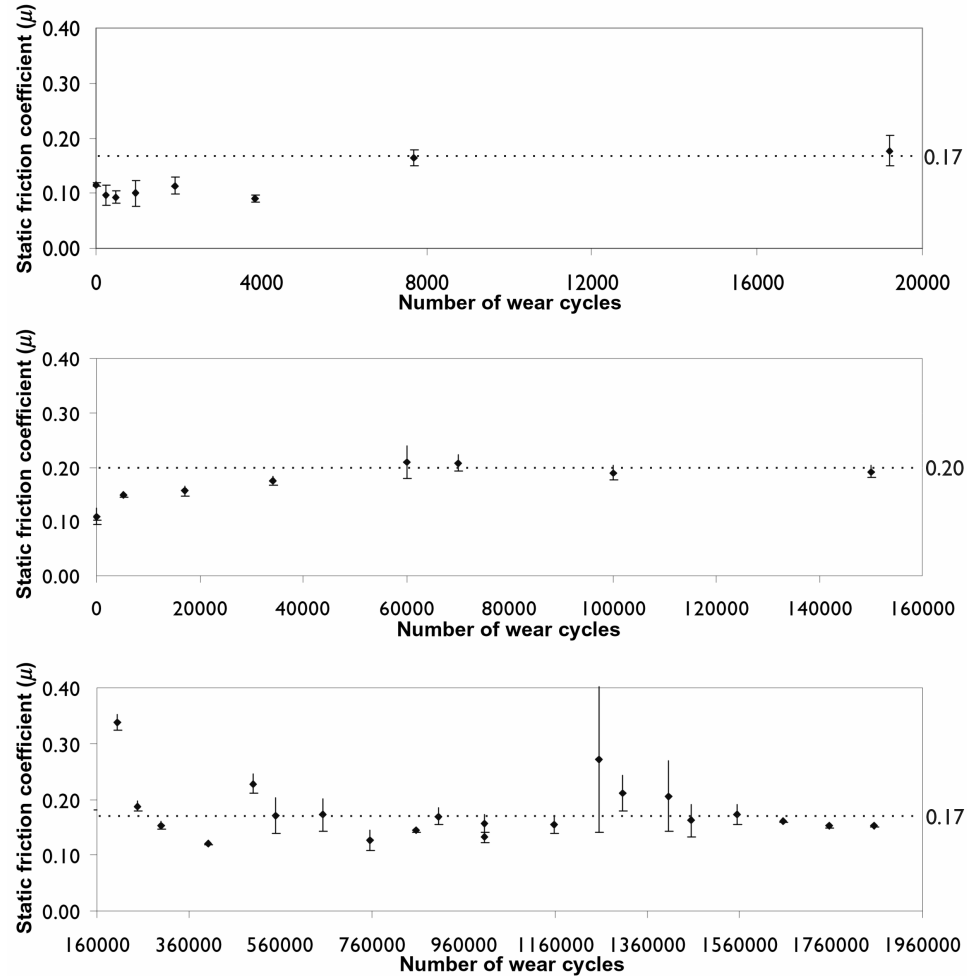
To gain additional insight in the wear mechanisms active in micron-scale silicon, static friction coefficients were measured at different points during the wear process. Friction data, where every data point is comprised of the average of 5-10 measurements, presented in Figure 4.19 shows an initial static coefficient of friction of  $\sim 0.11 \pm 0.01$ , which over the first 4,000 cycles stays approximately constant (Figure 4.19(a)). After  $\sim 20,000$  cycles it rises towards its steady state value of  $0.20 \pm 0.05$ , which it finally reaches at  $\sim 60,000$  cycles. Past 160,000 cycles the value of the coefficient of static friction shows an almost periodic fluctuation around a second steady-state value of  $\sim 0.17$ , with peaks up to  $\sim 0.30$ .

To acquire more insight with respect to the influence of the (worn) surface morphology and the wear mechanism on the value of the friction coefficient, a similar

friction/wear test was performed, where in this particular case after acquiring each value of the friction coefficient the worn surface of the device was observed using SEM. The friction data and accompanying wear surface overviews from this experiment are shown in Figure 4.20. As can be seen the values of the static coefficient of friction show a similar trend to the data in Figure 4.19. Specifically, it shows the increase from an initial value of  $\sim 0.11$  to a fluctuation around a steady state value slightly higher than 0.20. Interestingly enough, the accompanying SEM images of the surface, taken at different numbers of wear cycles, show that in a very early stage of the wear process (at  $< 27,000$  cycles) the first wear plowing track has already been created. This happened before the steady-state value of the static coefficient of friction was reached. This could suggest a decoupling of a changing wear mechanism and the fluctuations in values of the friction coefficient. It certainly shows that over almost the entire duration of the wear test an abrasive wear mechanism is active. In the first  $\sim 5000$  cycles the FDTD monolayer coating is expected to wear off of on the surface (other studies measuring friction coefficients in FDTD coated devices find a similar friction coefficient as the initial value in these tests [24]), followed by an increase in friction coefficient as first the thin ( $\sim 3$  nm) silicon oxide is removed before wear of the silicon commences.

From both the length scales of the features found in the electron microscopy studies in Section 4.3, summarized in Figure 4.16, as well as the IR and friction coefficient data presented in Section 4.4 and 4.5, the following wear mechanism can be deduced. Initially, a short adhesive regime occurs: first the monolayer coating wears away, followed by the silicon oxide. This creates freshly exposed silicon surfaces, which can come into contact and form strong bonds. This leads to a transition in wear

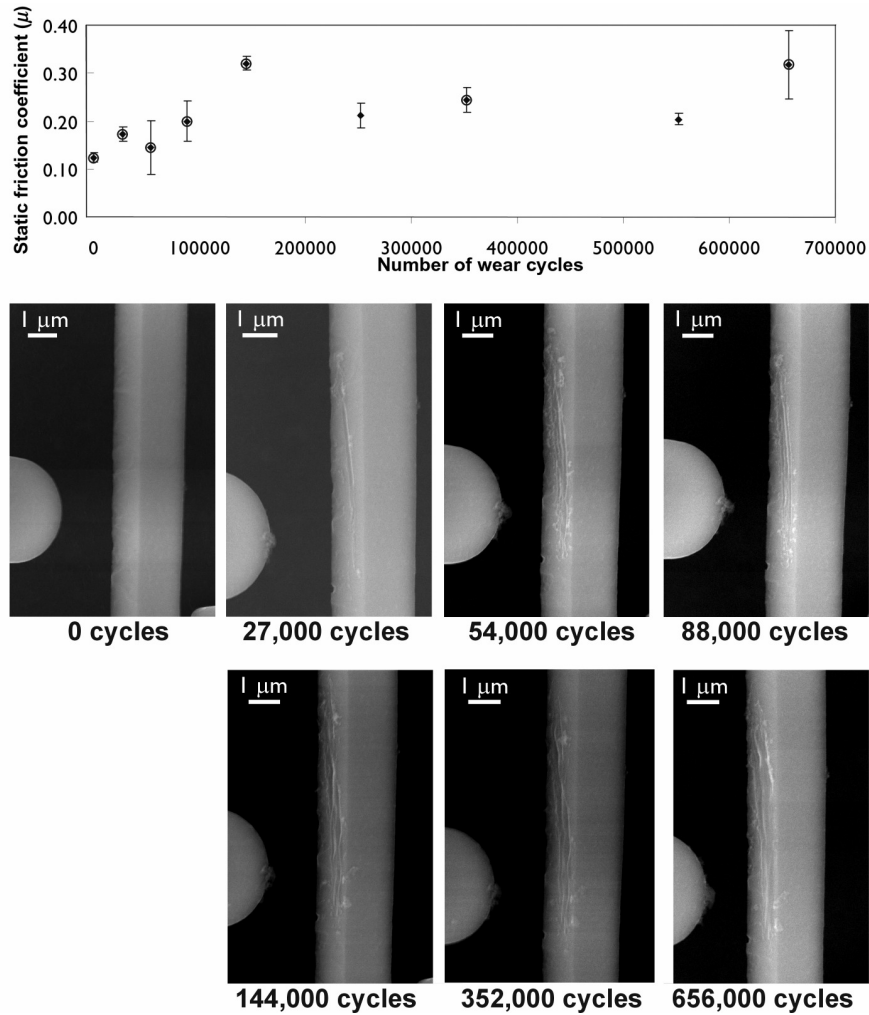
mechanism, to that of adhesive wear of silicon. These strong bonds between the two freshly exposed surfaces cause adhesive wear debris to be generated by fracture through the silicon grains. As soon as a critical mass of wear particles has been generated



**Figure 4.19:** Static coefficients of friction after different numbers of wear cycles (contact force  $\sim 3 \mu\text{N}$ ) in two devices (the lower two graphs are from the same test). After a short initial constant value, a higher steady-state value is reached; continuing wear causes a fluctuation around a slightly lower steady-state value beyond 160,000 cycles. The dotted lines in the graphs show the different steady-state regimes.

the governing wear mechanism switches from adhesive to third-body abrasive wear. In this regime, plowing tracks are created on the wear surface by the removal of more debris

particles (~50-100 nm with agglomerates up to ~500 nm) resulting from fracture through the grains (~500 nm). These wear debris particles oxidize heavily and become amorphous in the wear process. No evidence of plastic deformation of the silicon was found in any of these processes.



**Figure 4.20:** SEM silicon wear device surface morphology images during a wear experiment, showing the development of abrasive grooves in a very early stage of the wear experiment, which continue to increase in number as the wear process continues.

## 4.6 Summary and conclusions

*On-chip* polycrystalline silicon side-wall friction test specimens have been used to study active mechanisms in the sliding wear of polysilicon at micron-scale dimensions in ambient air. Wear debris and wearing surfaces were examined using analytical scanning and transmission electron microscopy and infrared microscopy. A summary of all the length scales of the different features encountered in these worn devices was given in Figure 4.16 and has been used to conclude how the wear particles were formed and their origin. Furthermore, measurement of the progression of the values of the static friction coefficient as wear progresses were performed and correlated with SEM worn surface overview images. From all these experiments the following wear mechanisms has been proposed: after a short (~5000 cycles) atomistic wear regime of the protective monolayer surface coating, the silicon oxide is worn away, creating freshly exposed silicon surfaces. Subsequent cycles result in wear particles being formed by adhesive wear. The adhesive wear regime only lasts for a short time (< 20,000-25,000 cycles), quickly being dominated by a third body abrasive wear regime, where silicon debris particles ~50-100 nm in size are created by abrasive wear from the initially created debris particles by fracture through the silicon grains (~500nm). All the wear particles subsequently oxidize and agglomerate into large (up to ~500 nm) debris clusters. This wear debris is amorphous (with a silica outer layer and a SiO<sub>x</sub> or potentially Si core). Plowing tracks are created on the worn surface by these hard debris particles and clusters, and are caused by cracking rather than plastic deformation. The exact composition of the debris particle core and the driving force for potential amorphization of the silicon debris is as of now unknown but it is likely caused by high local contact stresses. Concomitantly, a nano-

crystalline surface layer (thickness ~20-200 nm), with higher oxygen content than the rest of the beam (up to 35 atomic percent), forms during wear by partial oxidation of nano-crystalline silicon particles and the worn surface. These nano-crystals, which are smaller than debris particles found around the worn surface, are enclosed in this layer. Finally, IR microscopy revealed no evidence of significant temperature increases, nor did TEM show any dislocation pile-ups, ruling out any mechanisms that include (high-temperature) dislocation plasticity.

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## Chapter 5

# Summary and future work

### 5.1 Summary

Silicon is widely used in microelectromechanical systems (MEMS) applications. However, because of its brittle nature, it is clearly not an ideal structural material. Fatigue and wear in micron-scale polycrystalline silicon structural films can severely impact the durability and reliability of MEMS devices. Despite several studies on high-cycle fatigue behavior of these films, as well as studies on friction and wear in similar micron-scale films, there is still an on-going debate on the precise mechanisms involved in these two important failure modes.

#### 5.1.1 Fatigue of micron-scale silicon

Although bulk silicon is not susceptible to fatigue, micron-scale silicon has been demonstrated to display delayed failures under cyclic fatigue loading at applied cyclic stresses as low as half the (single-cycle) fracture strength. Since the early 1990s, several mechanisms to explain such fatigue failures in micron-scale silicon (both single and polycrystalline) have been suggested. These mechanisms can be divided into two main classes, namely those that attribute fatigue to a surface effect caused by cracking in the silicon-oxide layer and those that propose that subcritical cracking in the silicon itself is the cause of thin-film silicon fatigue.

Based on a review of the extensive literature on this topic, it is apparent that in general the stress-lifetime (S/N) fatigue data that have been measured by numerous authors all display similar trends, wherein lower cyclic stresses lead to a larger number of cycles to failure. Lifetimes are found to depend markedly on the environment, but not on loading frequency when considered in terms of cycles (and not time) to failure. It is argued that the published data from fatigue studies in both single and poly crystalline silicon present no convincing evidence to support the notion that the salient fatigue mechanisms involve subcritical cracking in the silicon itself. On the contrary, the majority of experimental evidence on micron-scale, thin-film silicon fatigue is consistent with the concept of a fatigue mechanism where subcritical cracking in the silicon oxide causes delayed failures.

In this work we have investigated the micron-scale very high-cycle fatigue ( $\sim 10^6$  to  $10^{12}$  cycles) of micron-scale polycrystalline silicon (free-standing) structural films (2-2.5  $\mu\text{m}$  thick) from two different fabrication sources (MUMPs and SUMMiT<sup>TM</sup>), tested in ambient air ( $\sim 25^\circ\text{C}$ , 30-40 %RH), high relative humidity air ( $>95$  %RH), and high vacuum ( $<2 \times 10^{-7}$  mbar) at  $\sim 36$ -40 kHz and a stress ratio of -1. High-frequency cyclic loading of micron-scale polysilicon thin films in ambient air result in premature fatigue failure after  $\sim 10^6$  to  $10^{12}$  cycles at applied maximum stresses less than the single-cycle fracture strength. S/N curves were obtained, with lifetimes in excess of  $\sim 10^{11}$  cycles when maximum stresses were typically  $\sim 70\%$  of the fracture strength. Such fatigue behavior in ambient air is observed in both MUMPs devices where the initial (post-release) oxide layers are large ( $\sim 15$ -30 nm), and in SUMMiT<sup>TM</sup> devices where the post-release oxide thicknesses are much smaller ( $\sim 3$ -6 nm). At a given applied (maximum)

stress, lifetimes are many orders of magnitude longer in the SUMMiT<sup>TM</sup> polysilicon films. Fatigue behavior, and hence corresponding device lifetimes, are highly sensitive to the test environment. Lifetimes are observed to be up to an order of magnitude shorter in a high-humidity atmosphere, as compared to ambient air. No fatigue failures could be induced for tests run *in vacuo*, even after cycling at stresses close to the fracture stress for more than  $10^{10}$  cycles.

For both MUMPs and SUMMiT<sup>TM</sup> devices, cumulative fatigue damage, which has been related to local oxidation and subcritical cracking, could be detected throughout fatigue testing by a progressive decay in the resonant frequency of the device. Such behavior has always been seen for tests in air, but never for tests *in vacuo* where no changes in resonance could be detected. High-voltage and energy-filtered transmission electron microscopy (TEM) imaging of the silicon oxide layers after cycling confirm the occurrence of thickening of the oxide films, typically by 4 to 6 times, in the locally high stress region in the vicinity of the notch. Such behavior is not observed after cycling *in vacuo*.

These fatigue results show conclusively that the reaction-layer fatigue mechanism for fatigue failure of micron-scale silicon films, where cyclic stress-induced delayed failures can occur at stresses less than the (single-cycle) fracture strength due to moisture-induced subcritical (stable) cracking within the oxide layer, is the governing mechanism for fatigue of micron-scale silicon. This mechanism is specific to thin-film silicon where cracks within the oxide can reach a large enough size to cause catastrophic failure of the entire device.

### 5.1.2 Wear of micron-scale silicon

*On-chip* polycrystalline silicon side-wall friction MEMS test specimens from the SUMMiT™ process were used to study active mechanisms during sliding wear in micron-scale silicon in ambient air. Worn parts are examined by analytical scanning electron microscopy (SEM) and TEM, while local temperature changes are monitored using advanced infrared (IR) microscopy. Furthermore, measurement of the progression of the values of the static friction coefficient as wear progresses were performed and correlated with SEM worn surface overview images.

Observations show that small amorphous debris particles (~50-100 nm) are removed by fracture through the silicon grains (grain size ~500 nm) and are oxidized and amorphized during this process, yielding a silica outer layer and an SiO<sub>x</sub> or potentially amorphous silicon core. The exact composition of this core as well as the driving force for the potential amorphization of the silicon debris is as of now unknown but is likely caused by high local contact stresses. Agglomeration of such debris particles into larger clusters also occurs. Some of these debris particles/clusters create plowing tracks on the beam surface. Concomitantly, a nano-crystalline surface layer (thickness ~20-200 nm), with higher oxygen content than the rest of the beam (up to 35 atomic percent), forms during wear by partial oxidation of nano-crystalline silicon particles at the worn surface. These nano-crystals, which are smaller than debris particles found around the worn surface, are enclosed in this layer. IR microscopy revealed no evidence of significant temperature increases, nor did TEM show any dislocation pile-ups, ruling out any mechanisms that include (high-temperature) dislocation plasticity. The values of static coefficients of friction reach a steady-state value of  $\sim 0.20 \pm 0.05$  early in the test after a

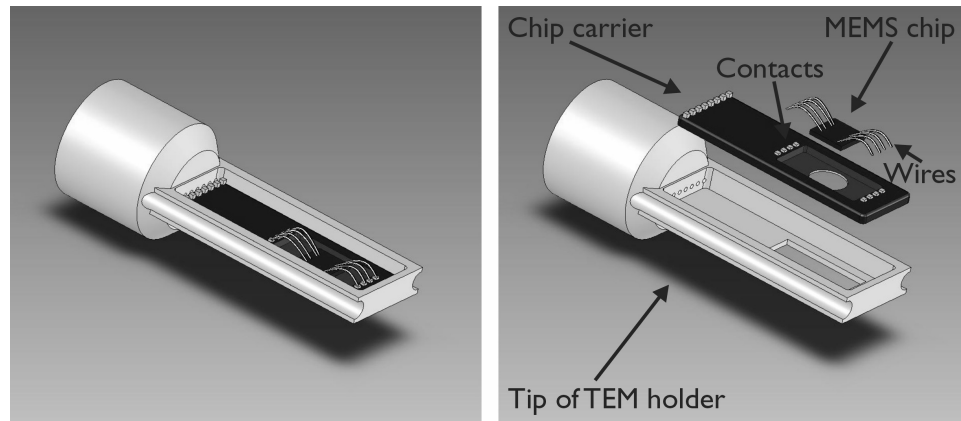


short time of the initial value of  $\sim 0.11 \pm 0.01$ . This transition is only partly coupled to the change in wear mechanism from a short adhesive regime, allowing the first debris particles to be formed, to a third body abrasive regime, because the first plowing tracks are seen before the friction coefficient reaches its steady-state value ( $\sim 0.20 \pm 0.05$ ). This evidence suggests the following active wear mechanisms: after a short ( $\sim 5000$  cycles) atomistic wear regime of the protective monolayer surface coating the silicon oxide is worn away, creating freshly exposed silicon surfaces, which create some wear particles by adhesive wear. The adhesive wear regime only lasts for a short time ( $< 20,000$ - $25,000$  cycles), quickly being dominated by a third body abrasive wear regime.

## 5.2 Future Work

Although the reaction-mechanism seems the most likely candidate for fatigue in micron-scale silicon, the cause of the cyclic stress-assisted oxidation process, observed by TEM after fatigue failure, but not after overload fracture failure, or cyclic loading in vacuum, remains unknown. Imaging this process as it is happening could reveal the origin of this oxide thickening phenomenon. It would also prove the reaction-layer mechanism's validity even more conclusively. Direct bright field observations of this cyclic stress-assisted oxide thickening phenomenon could be made by running a fatigue test *in-situ* inside a TEM. In order to allow this, an appropriate TEM holder is needed that fits a MEMS chip containing fatigue testing devices and also allows biasing of the chip inside the TEM column, while imaging. A conceptual drawing of such a holder is shown in Figure 5.1. Because a high vacuum environment does not produce fatigue failure, an environmental TEM (E-TEM) would be needed, which would automatically allow the

observation of the influence of running tests in different types of environments, like oxygen and nitrogen. Furthermore, to allow electron beam transparency, a MEMS chip needs to be fabricated with structural silicon film thicknesses in the 100's of nm range (as opposed to the  $\sim 2\text{ }\mu\text{m}$  films used in the studies presented in Chapter 3 and 4), as well as with a backside etched hole to allow the electron beam to get past the substrate after it has traveled through the silicon structural film. Finally because of the lack of space between the pole pieces in the electron microscope where the specimen will sit, this entire setup cannot be more than  $\sim 4\text{ mm}$  high, and this included the wire bonding that connects the contacts on the chip package with the contact pads on the MEMS chip. A setup like this should allow *in-situ* observation of the fatigue process by bright field imaging as it is occurring and can provide insight into the origin of the cyclic stress-assisted oxidation.



**Figure 5.1:** TEM in-situ MEMS biasing holder design concept.

A final note on fatigue of silicon has to be made with respect to trends of fabricating even smaller silicon structures for nanoelectromechanical systems (NEMS). At these length scales, critical crack sizes for fracture decrease even more. Since the

thickness of native oxide layer does not scale significantly when changing the length scales of silicon features, fatigue will become even more of a reliability issue when structures become even smaller. In the near future, knowledge of fatigue in silicon and particularly at smaller size scales (sub-micrometer level) will be needed to allow successful NEMS fabrication. Only when reliability issues in these nano-scale systems can be solved will nano-science be able to become successful nano-technology.

Next to expanding the knowledge of wear mechanisms in micron-scale silicon to different operating environments (vacuum, different humidities, oxygen or nitrogen environments), more quantitative knowledge about wear in micron-scale silicon can also be obtained by measuring wear volumes. Atomic force microscope (AFM) measurements could be performed on specimens prepared using focused ion beam (FIB) (to allow scanning of the worn sidewalls, which would otherwise be unreachable for the AFM tip). This would allow wear volumes to be determined and correlated with the wear conditions, specifically the number of cycles and load. These quantitative measurements can be used to compare to known wear trends from macro-scale applications for known mechanisms, where depending on wear conditions the value of the wear rate for micrometer scale contacts is reported to be:  $10^{-14}$  to  $10^{-12}$  m<sup>3</sup>/(N.m) [1,2]. Specifically, Archard's law:

$$V_w = \frac{k}{3} \frac{xL}{p} \quad (5.1)$$

where  $V_w$  is the worn volume,  $k$  the wear coefficient,  $x$  sliding length,  $L$  normal force between surfaces,  $p$  hardness, one of the basic relationships describing adhesive and

abrasive wear of materials, can be verified (or modified) for micron-scale dimensions. This will allow accurate prediction of wear rates for future applications, which will make designing reliable silicon MEMS more achievable.

### 5.3 References

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## Appendix A

# Micron-scale fatigue testing methods

The micron-scale silicon fatigue test results presented in Section 2.2 and 2.3 have been obtained using several different testing configurations. In this appendix, the increasing variety of testing methods that have been used to study such thin-film fatigue are illustrated. Currently two major classes of testing systems can be distinguished: (i) *on-chip* electrical testing systems, where the tested structural film and the electrostatic actuation is integrated onto a MEMS chip (most of these testing systems use electrostatic actuation), and (ii) testing systems where the micron-scale test sample is separated from a larger scale external actuator.

### A1: On-chip electrically-actuated loading systems

The first micron-scale fatigue characterization structure used by Connally and Brown [1,2,3] comprised a micromachined p-type single-crystal silicon cantilever beam (pre-cracked) attached to a rectangular plate allowed to electrostatically resonate in the out-of-plane direction. Van Arsdell and Brown [4] developed a similar fatigue testing procedure for polysilicon, again using electrostatically-actuated devices, but with the difference that in-plane rather than out-of-plane resonance was used. Their fatigue characterization structures consisted of a 2  $\mu\text{m}$  thick cantilever beam (pre-cracked) attached to a triangular-shaped proof mass fabricated in the MEMSCAP (then MCNC) MUMPs process [5,6]. Muhlstein, Brown, and Ritchie (Figure 2.2 [7]) utilized the same

design for their single-crystal boron doped silicon testing, although instead of using pre-cracked beams to investigate crack propagation [1,4], they employed a notched cantilever beam (with a 1  $\mu\text{m}$  root radius) to permit the investigation of both initiation and growth of small flaws. Muhlstein, Brown, Stach and Ritchie [8-11] and Shrotiya, Allameh, Soboyejo and coworkers [12-15] also used this resonator design for the testing of thin-film polysilicon. Their specimens (2  $\mu\text{m}$  thick,  $n^+$ -type polysilicon, also fabricated in the MUMPs foundry [5,6]) again consisted of a notch cantilever beam (without pre-crack) attached to a triangular-shaped proof mass that was electrostatically actuated at resonance; displacements were measured using capacitive sensing. Pierron and Muhlstein [16] used  $n^+$ -type single-crystal silicon (10  $\mu\text{m}$  thick) resonators, fabricated in the MEMSCAP SOIMUMPs process<sup>6</sup>, again based on the design by Van Arsdell and Brown [4].

Several other resonator designs have been used to investigate thin-film silicon fatigue. Tabib-Azar *et al.* [17] utilized heavily doped ( $p^+$ -type) micromachined single-crystal silicon cantilever beams (not pre-cracked), which were electrostatically excited at resonance at a frequency of  $\sim 6\text{-}7$  kHz ( $R = -1$ ). An optical deflection system was used to measure the deflection angle, and hence the displacements (for small deflection angles), of the cantilever beam. Koskenvuori *et al.* [18] used 10  $\mu\text{m}$  thick single-crystal silicon micro-resonators which they actuated in length-extensional mode. The resonators consisted of a 145  $\mu\text{m}$  long arm with a resonant frequency  $f_0 = 13.1$  MHz (electrostatically actuated at  $R = -1$ ).

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<sup>6</sup> More information: <http://www.memscap.com/memsrus/svcsoirules.html>

Yet another specimen design was used by Kahn, Ballarini, and Heuer [19-22] who developed electrostatically-actuated polysilicon fatigue specimens that offered the unique ability to perform cyclic loading (at resonance) at varying loading ratios ( $-3 < R < 0.5$ ), by superposing a DC voltage to an AC voltage. The device consisted of two, large, interdigitated comb drives; one comb drive was free to move in the plane of the structure when subjected to electrostatic actuation. Attached to this comb drive was a notched beam (anchored to the substrate on one end) with a  $1\text{ }\mu\text{m}$  root radius notch used for stress concentration (Figure 2.6). The devices were fabricated from a  $5.7\text{ }\mu\text{m}$  thick film of polysilicon that was doped with boron. They also used an alternate device consisting of undoped polysilicon coated with  $\sim 10\text{ nm}$  of palladium (Pd) for sufficient conductivity; the tensile residual stress associated with the Pd coating allowed the devices to be driven at resonance, while the displacement was measured optically.

Ferraris *et al.* [23] also used an electrostatic actuator device which comprised an electrostatic comb driven reciprocal rotor actuator, similar to the design used by White *et al.* [24]; this permitted fully reversed bending loading on an unnotched beam. A different type of polysilicon actuator was employed by Kapels, Aigner and Binder [25], consisting of an electrically powered thermal actuator. Their actuator consisted of two narrow beams (of different lengths) that expanded due to electrical heating, and a cold plate to which a short beam (the specimen) was attached. A sinusoidal current was used to generate tension-tension cyclic loading ( $R = 0$ ) at a frequency of  $1\text{ Hz}$ , and displacements were measured optically.

## A2: Externally-actuated loading systems

An external piezoelectric actuated resonator involving single-crystal silicon resonators was utilized by Tsuchiya and coworkers [26]. The test device was bulk micromachined and consisted of a mass supported by four beams (the test specimens) connected with strain gauges that measured the vertical displacement of the mass. The resonant frequency of the device was about 9 kHz. The resonator was oscillated using a piezoelectric actuator ( $R = -1$ ) in a closed-loop configuration that allowed testing at resonance at constant amplitude. Another type of specimen and external actuation method was utilized by Komai, Minoshima, and coworkers [27,28], which involved single-crystal silicon cantilever beams. These tests were performed using a specially designed electromagnetic actuator, allowing tension cyclic loading ( $R = 0.1$ ) at a frequency of 0.1 Hz. Displacements were measured using a differential transformer. Ando *et al.* [29] used a tensile testing method. Their micromachined single crystal device consisted of a tensile specimen attached to a load lever, a pair of torsion bars and the supporting frame. An external load applied perpendicularly to the loading lever resulted in uniaxial loading of the tensile specimen. Cyclic loading was performed at 10 Hz under displacement control with a stress ratio,  $R$ , of 0.1.

Fatigue testing at small dimensions was achieved by Sundurarajan and Bushan [30] who used single-crystal silicon nanometer-scale double clamped beams fabricated from a {100} silicon-on-insulator wafer. They employed an AFM to bend the beams while monitoring loads and displacements. Another study using AFM actuation was performed by Namazu and Isono, who employed different types of micron-scale single-crystal silicon specimens [31,32], specifically, nano-scale fixed-fixed beams (width < 1



$\mu\text{m}$ , thickness 255 nm, length 6  $\mu\text{m}$ ) with trapezoid-shape cross-section and various micron-scale specimens for bending and tensile mode testing. Fatigue tests were performed using an AFM (for nano-scale specimens), a nano-indentation tester (for micron-scale bending specimens), or a compact tensile tester manufactured by the authors (for micron-scale tensile specimens). The stress ratio was positive (cyclic tension loading) and the loading frequency ranged from 10 Hz to 450 Hz.

A very different method was used by Dauskardt, Kenny, Fitzgerald, and coworkers, who utilized single-crystal silicon micromachined specimens with a 150  $\mu\text{m}$  thick test section (Figure 2.3 [33,34]). A compression-loaded double cantilever-beam specimen with an external load was used to produce stable controlled-growth tensile crack. Crack growth was measured via change in electrical resistance of a thin metal film deposited on the side face of the specimen, with a thin oxide layer in between. Specimens were tested under monotonic loading in both displacement and load control. A sharp pre-crack was initially formed from the blunt notch. Cyclic tests were run at 20 Hz with an applied sinusoidal waveform and nominal stress ratio  $R = 0.1$ .

Finally, Bagdahn and Sharpe (Figure 2.15 [35-37]) investigated externally actuated micro-tensile specimens, with applied stresses directly measured using an external load cell. The specimens were loaded with a low voltage piezoelectric actuator for frequencies up to 1 kHz, or with a loudspeaker at 6 kHz, under zero-tension cyclic loading (i.e., at  $R = 0$ ).

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## Appendix B

# Oxidation models for Silicon

The “native oxide” of silicon is the very thin oxide that grows spontaneously on a clean silicon surface exposed in an ambient environment. After several days, the native oxide typically is around 20 Å, depending on preparation conditions, whereas the formation of the first 5-10 Å of oxide on a silicon surface in air or water can be as quick as a few minutes [1,2]. Although a lot of research on this particular topic exists, the mechanism responsible for native oxide formation is not fully understood [3]. The mechanism should have a strong electrochemical nature and the diffusion of oxygen through the oxide is the limiting step as far as supplying the reaction species is concerned. Models that deal with oxidation are usually argued from a thermal oxidation (i.e. oxidation at elevated temperature) point of view, because of its processing importance. However, these physical concepts can also be applied at room temperature, where the process will be slower and reach a different point of equilibrium.

### B.1 The Deal-Grove model

Extensive research on the oxide film growth on silicon has been performed because of its aforementioned technological importance in the integrated-circuit industry. The first model was published by Deal and Grove in the mid 1960's [4]. In the 1980's, Irene [5] and Fargeix et al. [6] proposed additional models to explain the high oxidation rate of

dry oxidation (in air, often at high (~700-1200 °C) temperatures) for very thin oxides (< 30 nm). These models include the contribution of intrinsic stresses that develop at the silicon/oxide interface.

The Deal - Grove model [4,7] assumed three steps occurring in series:

1. Reaction and adsorption of oxidizing gas to the outer surface of the oxide
2. Fickian diffusion of oxidants (molecular water or oxygen) through the existing oxide layer toward the silicon/oxide interface. Here Fick's model for diffusion of solutes in solution is applied to a gas diffusing through a solid
3. First order chemical reaction at the interface

The fluxes  $F_1$ ,  $F_2$ , and  $F_3$ , associated with the three respective steps are given by Equation (B.1), (B.2), and (B.3):

$$F_1 = h(C^* - C_0) \quad (B.1)$$

$$F_2 = D_{eff} \frac{C_0 - C_{int}}{x_0} \quad (B.2)$$

$$F_3 = kC_{int} \quad (B.3)$$

with  $h$  the gas transport coefficient,  $C^*$  the equilibrium concentration of the oxidant (oxygen or moisture) in the oxide,  $C_0$  the oxidant concentration at the outer surface of the oxide,  $D_{eff}$  the effective diffusion coefficient,  $C_{int}$  the concentration of the oxidant near the silicon/oxide interface,  $x_0$  the oxide thickness, and  $k$  chemical rate constant for the oxidation reaction. Assuming all three fluxes are equal, Equation (B.4) can be obtained:

$$x_0^2 + Ax_0 = B(t + \tau) \quad (B.4)$$

with  $A$  given by Equation (B-5):

$$A = 2D_{eff} \left( \frac{1}{k} + \frac{1}{h} \right) \quad (B.5)$$

and  $B$  given by Equation (B.6):

$$B = \frac{2D_{eff}C^*}{N_1} \quad (B.6)$$

with  $N_1$  is the number of oxidant molecules per unit volume of oxide. The quantity  $\tau$  corresponds to a shift in time coordinate to account for the initial oxide layer prior to thermal oxidation.

There are two limiting forms of the solution that are of particular interest. For long oxidation times, i.e. thick oxide layers, Equation (B.4) can be reduced to Equation (B.7):

$$x_0^2 \approx Bt \quad (B.7)$$

which corresponds to the parabolic oxidation law for long times. Therefore  $B$  is known as the parabolic rate constant. For short times, or thin oxide layers, Equation (B.4) can be reduced to Equation (B.8):

$$x_0 \approx \frac{B}{A}(t + \tau) \quad (B.8)$$

Equation (B.4) therefore reduces to a linear law, and the coefficient  $B/A$  is known as the linear rate constant. Equation 4, along with the two limiting forms Equation (B.7) and Equation (B.8), successfully fitted experimental data over a wide range of variables [4,7].

An exception of the good agreement between experimental data and the Deal – Grove model was encountered in the case of “very thin” oxide regime (< 30 nm) at “low” temperatures (700 – 1000 °C) for dry oxidation. As experimental data has shown, an

initial high oxidation rate occurs prior to reaching the limiting form given by Equation (B.8). This result suggested that a different mechanism of oxidation could be active for oxide thicknesses lower than  $\sim 30$  nm.

The formation of silicon-oxide during thermal oxidation usually results in compressive stresses in the oxide layer. The oxide molar volume ( $27 \text{ cm}^3/\text{mol}$ ) is larger than the silicon molar volume ( $12 \text{ cm}^3/\text{mol}$ ) it replaces, creating compressive stress upon oxide formation. Below  $1000^\circ\text{C}$ , the large compressive interfacial stresses do not relax due to the high viscosity of the oxide [8]; therefore low oxidation temperatures usually result in large compressive stresses within the oxide layer. As will be shown below, these stresses have a negative influence on the possibility of diffusion of oxygen and water through the oxide layer. This can be conceptually understood knowing that with a compressive stress in the oxide layer the lattice spacing will be slightly smaller and given the fact that the oxygen and water diffuse interstitially.

## B.2 The “stress-stated” model

Several models tried to explain the high rate regime through an enhancement of the diffusivity of the oxidants [5]. In contrast, Fargeix *et al.* [6,9,10] suggested that a decrease of the diffusivity,  $D_{eff}$  in Equation (B.2), could account for the initial high rate regime in dry oxidation at low temperatures. Their “stress-stated” model involved the following:

1. Deal – Grove process (diffusion of the oxidizing species and reaction at the silicon/oxide interface).



2. Decrease in diffusivity of the oxidants due to high compressive stress.
3. Stress relief mechanism due to viscous flow.

This model relied on experimental evidence suggesting a decrease on the grown oxide thickness at the location of local compressive stress [6]. A physical reason for a decrease in diffusivity with compressive stress is based on an increase in steric hindrance [10] due to compressive stress.

Fargeix *et al.* used the following expression for diffusivity under stress (Equation (B.9)):

$$D = D_0 e^{\left(\frac{-\sigma\Delta V}{kT}\right)} \quad (\text{B.9})$$

with  $\sigma$  the stress level,  $\Delta V$  the diffusion volume change due to stress, and  $D_0$  the diffusivity for the unstressed oxide, given by Equation (B.10):

$$D_0 = D_{00} e^{\left(\frac{-E_a}{kT}\right)} \quad (\text{B.10})$$

with  $E_a$  the formation energy for dry thermal silicon-oxide. Therefore the parabolic constant  $B$  (see Equation (B.6)) is given by Equation B.11:

$$B = B_0 e^{\left(\frac{-E_a + \sigma\Delta V}{kT}\right)} \quad (\text{B.11})$$

where  $\Delta V$  can be approximated with Equation (B.12):

$$\Delta V = \frac{V_0}{K} \sigma \quad (\text{B.12})$$

with  $V_0$  the specific volume of the oxide and  $K$  the compressibility of silica [10,7].

### B.3 Irene's model

The model described in the previous section handles the influence of stress through the parabolic constant,  $B$ . Instead, Irene proposed a modified model based on a change in the linear kinetic constant,  $k$ , with stress [5,7]. His model incorporated the following modifications:

1. A new mode for oxidant transport through micro-pores;
2. Strain effects on the interface reaction.

Irene obtained an expression for the flux of the oxygen or water molecule going through the micro-pores (Equation B.13):

$$F_{2,micropores} = \frac{\lambda(C_0 - C_{int})}{x_0} N_p \quad (B.13)$$

with  $\lambda$  a constants,  $x_0$  the oxide thickness (equal to the length of the micro-pores), and  $N_p$  the number of pores, which is assumed to decrease with increasing oxide thickness. This flux is only dominant over the flux associated with diffusion (Equation B.2) for very thin oxide layers. In that case, the micro-pores length is approximately equal to the oxide thickness. Irene also explained the high oxidation rate associated with low oxidation temperature and very thin oxide thickness (for dry oxidation) through the influence of intrinsic stresses on the interface reaction. The compressive stresses developing in the growing oxide generate tensile stresses at the silicon surface. Irene suggested that the first order chemical rate constant for the oxidation reaction,  $k$ , depends on the available number of silicon atoms at the silicon/oxide interface [5]. The modified flux,  $F_3$ , with respect to Equation (B.3), is given by Equation B.14:

$$F_3 = \left( k' \frac{C_{Si} \sigma}{\eta} \right) C_{\text{int}} \quad (\text{B.14})$$

with  $k'$  the rate constant,  $C_{Si}$  the a real density of silicon atoms on a given surface,  $\sigma$  the tensile stress at the silicon surface, and  $\eta$  the viscosity of the oxide. This equation suggests that high tensile stresses can increase the rate of the chemical reaction at the interface, therefore increasing the overall oxidation rate.

This appendix presented three models proposed for oxidation and showed that the thermal oxidation of silicon is affected by the presence of stresses that arise from the formation of silicon-oxide. The compressive stresses within the oxide decrease the diffusivity of the oxygen or water molecules [10], while the corresponding tensile stresses within silicon accelerate the chemical reaction at the silicon/oxide interface [5]. The micro-pores present within very thin (< 30 nm) oxide layers could also increase the flux of oxygen or water molecules reaching the silicon/oxide interface [5].

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# Appendix C

## Publications

### Chapter 2

Mechanisms For Fatigue Of Micron-Scale Silicon Structural Films

D.H. Alsem, O. Pierron, E.A. Stach, C.L. Muhlstein and R.O. Ritchie

*Advanced Engineering Materials, accepted, November 2006*

### Chapter 3

*Fatigue Failure In Thin-Film Polycrystalline Silicon Is Due To Subcritical Cracking*

*Within The Oxide Layer*

D.H. Alsem, E.A. Stach, C.L. Muhlstein and R.O. Ritchie

*Applied Physics Letters, vol 86, Jan 2005, pp. 41914-1-3*

*Very High-Cycle Fatigue Failure In Micron-Scale Poly-Crystalline Silicon Films: Effects*

*Of Environment And Surface Oxide Thickness*

D.H. Alsem, R. Timmerman, B.L. Boyce, E. A. Stach, J. Th. M. de Hosson and R.O.

Ritchie

*Journal of Applied Physics, accepted, October 2006*

## Chapter 3/4

*Utilizing On-Chip Testing And Electron Microscopy To Obtain A Mechanistic*

*Understanding Of Fatigue And Wear In Polysilicon Structural Films*

D.H. Alsem, E.A. Stach, C.L. Muhlstein, M.T. Dugger, and R.O. Ritchie

*Materials Research Society Meeting Proceedings, April 2004.*

*Wear And Fatigue In Silicon Structural Films For Mems Applications*

D.H. Alsem, R. Timmerman, E.A. Stach, M.T. Dugger and R. O. Ritchie

*Proceedings of the European Conference of Fracture (ECF16), July 2006*

## Chapter 4

*An Electron Microscopy Study Of Wear In Polysilicon Microelectromechanical Systems*

D.H. Alsem, E.A. Stach, M.T. Dugger, Marius Enachescu and R.O. Ritchie

*Journal of Thin Solid Films, in-press, February 2006*